

MS-7407 Ver : 0A

Intel (R) LGA775 Processor (130W)

Intel (R) (GMCH G31) + ICH7 Chipset

CPU:

Intel Core 2 Duo/Extreme/Quad & Pentium D Processor

System Chipset:

Intel G31 (North Bridge) Rev : A2

Intel ICH7 (South Bridge) Rev : A1

On Board Chipset:

CLOCK : ICS9LP505

PCIE LAN 82573L

LPC Super I/O : W83627DHG Ver :

DVI : CHRONTEL/CH7307C

Audio Codec : ALC888 7.1 Channel Ver : A1

BIOS : SPI- 8M

Main Memory:

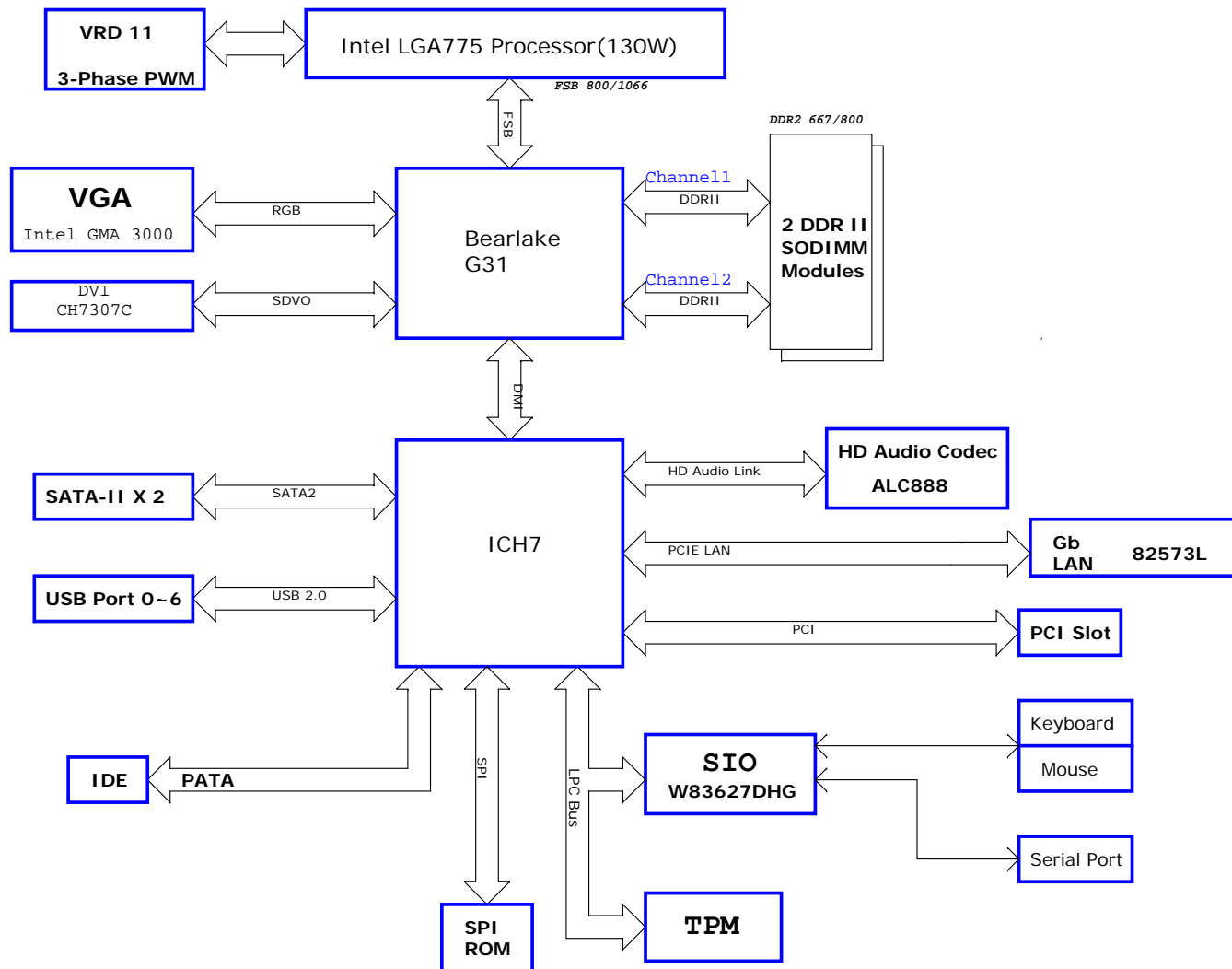
DDR II * 2 (Max 4GB)

Expansion Slots:

PCI X SLOT *1 (FOR PCI Riser)

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Block Diagram



Micro Star Restricted Secret		
Title	BLOCK DIAGRAM	Rev 20
Document Number	MS-7407	
MICRO-STAR INT'L CO., LTD. No. 66, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, August 27, 2007 Sheet 2 of 36

ICH7

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	ToI	Default	Signal Name
GPIO[0]	BM_BUSY#	AB18	I/O	Vcc3p3	N	Y	3.3	Input	strapped high
GPIO[1]	PCIREQ[5]#	C8	I/O	V5REF	N	Y	5	Input	PREQ#5
GPIO[2]	PIRQE#	G8	I/OD	V5REF	N	Y	5	Input	PIRQ#E
GPIO[3]	PIRQF#	F7	I/OD	V5REF	N	Y	5	Input	PIRQ#F
GPIO[4]	PIRQG#	F8	I/OD	V5REF	N	Y	5	Input	PIRQ#G
GPIO[5]	PIRQH#	G7	I/OD	V5REF	N	Y	5	Input	PIRQ#H
GPIO[6]	unmuxed	AC21	I/O	Vcc3p3	N	Y	3.3	Input	ATADET0
GPIO[7]	unmuxed	AC18	I/O	Vcc3p3	N	Y	3.3	Input	strapped high
GPIO[8]	unmuxed	E21	I/O	VccSus3p3	N	Y	3.3	Input	SIO_PME#
GPIO[9]	unmuxed	E20	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[10]	unmuxed	A20	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[11]	SMBALERT#	B23	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[12]	unmuxed	F19	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[13]	unmuxed	E19	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[14]	unmuxed	R4	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[15]	unmuxed	E22	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[16]	unmuxed	AC22	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[17]	PCIGNT[5]#	D8	I/O	Vcc3p3	N	N	3.3	N/A	PGNT#5
GPIO[18]	unmuxed	AC20	I/O	Vcc3p3	N	N	3.3	1	SPI_HOLD#
GPIO[19]	SATA1GP	AH18	I/O	Vcc3p3	N	N	3.3	Input	strapped high
GPIO[20]	unmuxed	AF21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[21]	SATA0GP	AF19	I/O	Vcc3p3	N	N	3.3	Input	strapped high
GPIO[22]	PCIREQ[4]#	A13	I/O	Vcc3p3	N	N	3.3	Input	PREQ#4
GPIO[23]	LDRQ1#	AA5	I/O	Vcc3p3	N	N	3.3	Input	NC
GPIO[24]	unmuxed	R3	I/O	VccSus3p3	N	N	3.3	No Change	LAN_DIS#
GPIO[25]	unmuxed	D20	I/O	VccSus3p3	Y	N	3.3	1	DMI_MODE
GPIO[26]	unmuxed	A21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[27]	unmuxed	B21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[28]	unmuxed	E23	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC5#	C3	I/O	VccSus3p3	N	N	3.3	Input	USB_OCP#4
GPIO[30]	OC6#	A2	I/O	VccSus3p3	N	N	3.3	Input	USB_OCP#4
GPIO[31]	OC7#	B3	I/O	VccSus3p3	N	N	3.3	Input	USB_OCP#4
GPIO[32]	unmuxed	AG18	I/O	Vcc3p3	N	N	3.3	1	SPI_WP#
GPIO[33]	unmuxed	AC19	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[34]	unmuxed	U2	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[35]	unmuxed	AD21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[36]	SATA2GP	AH19	I/O	Vcc3p3	N	N	3.3	Input	strapped high
GPIO[37]	SATA3GP	AE19	I/O	Vcc3p3	N	N	3.3	Input	strapped high
GPIO[38]	unmuxed	AD20	I/O	Vcc3p3	N	N	3.3	Input	strapped high
GPIO[39]	unmuxed	AE20	I/O	Vcc3p3	N	N	3.3	Input	strapped high
GPIO[48]	GNT4#	A14	I/O	Vcc3p3	N	N	3.3	N/A	PGNT#4
GPIO[49]	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	CPU	N/A	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD20	PCI_CLK1
PCI Slot 2	PIRQ#C PIRQ#D PIRQ#A PIRQ#B	PREQ#2 PGNT#2	AD21	PCI_CLK2
1394	PIRQ#B	PREQ#1 PGNT#1	AD19	1394_PCLK

PCI RESET DEVICE

Signals	Target
PCIRST#1	SIO,TPM
PCIRST#2	1394,DVI
PCIRST#3	PCI SLOT 1,2
PLTRST#	MS7
HD_RST#	Primary IDE

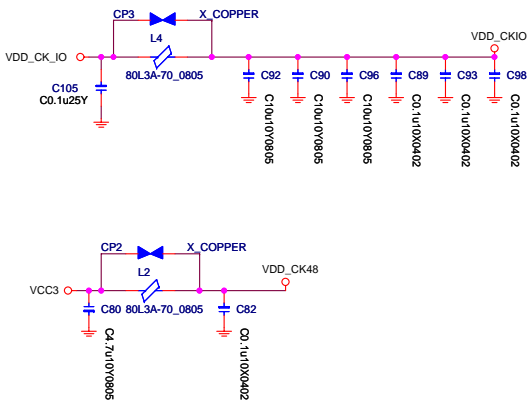
DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	SCLK_A0/SCLK_A#0 SCLK_A1/SCLK_A#1 SCLK_A2/SCLK_A#2
DIMM 2	A2H	SCLK_B0/SCLK_B#0 SCLK_B1/SCLK_B#1 SCLK_B2/SCLK_B#2

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
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Micro Star Restricted Secret			
Title	GPIO & Jumper Setting		Rev 20
Document Number	MS-7407		
MICRO-STAR INT'L CO.,LTD. No. 68, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, August 27, 2007 Sheet 3 of 36	



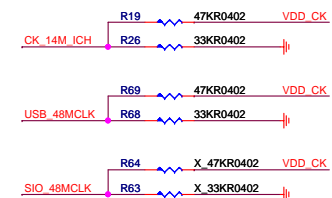
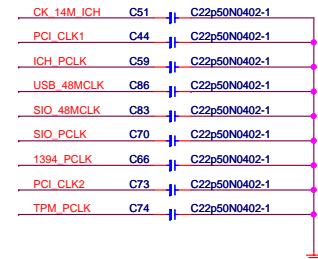
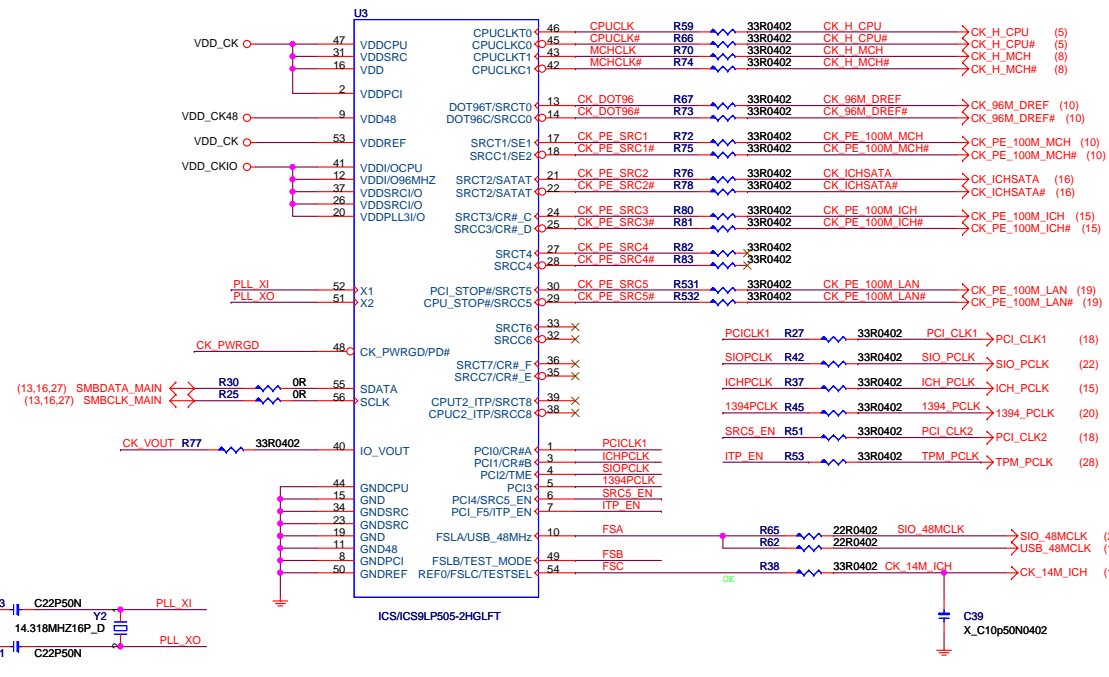
The diagram illustrates the VFSB_VTT power plane circuit. It features three 8P4R-470R0402 resistors (RN2, RN3, RN5) connected to a common VFSB_VTT supply. The connections are as follows:

- RN3 (8P4R-10KR0402):**
 - Pin 1: H_BSL0 (10)
 - Pin 3: H_BSL1 (10)
 - Pin 5: H_BSL2 (10)
 - Pin 4: Connected to VFSB_VTT
 - Pin 6: Connected to VFSB_VTT
- RN2 (8P4R-1KR0402):**
 - Pin 1: CPU_BSEL0 (5)
 - Pin 3: CPU_BSEL1 (6)
 - Pin 5: CPU_BSEL2 (5)
 - Pin 4: Connected to VFSB_VTT
 - Pin 6: Connected to VFSB_VTT
- RN5 (8P4R-470R0402):**
 - Pin 1: Connected to VFSB_VTT
 - Pin 3: Connected to VFSB_VTT
 - Pin 4: FSA (5)
 - Pin 6: FSB (5)
 - Pin 7: FSC (5)

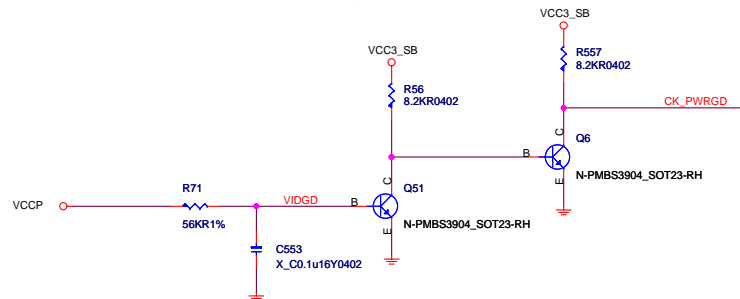
Green labels (10) and (5) indicate signal levels or bus widths. The VFSB_VTT supply is shown at the top, and the ground reference is at the bottom.

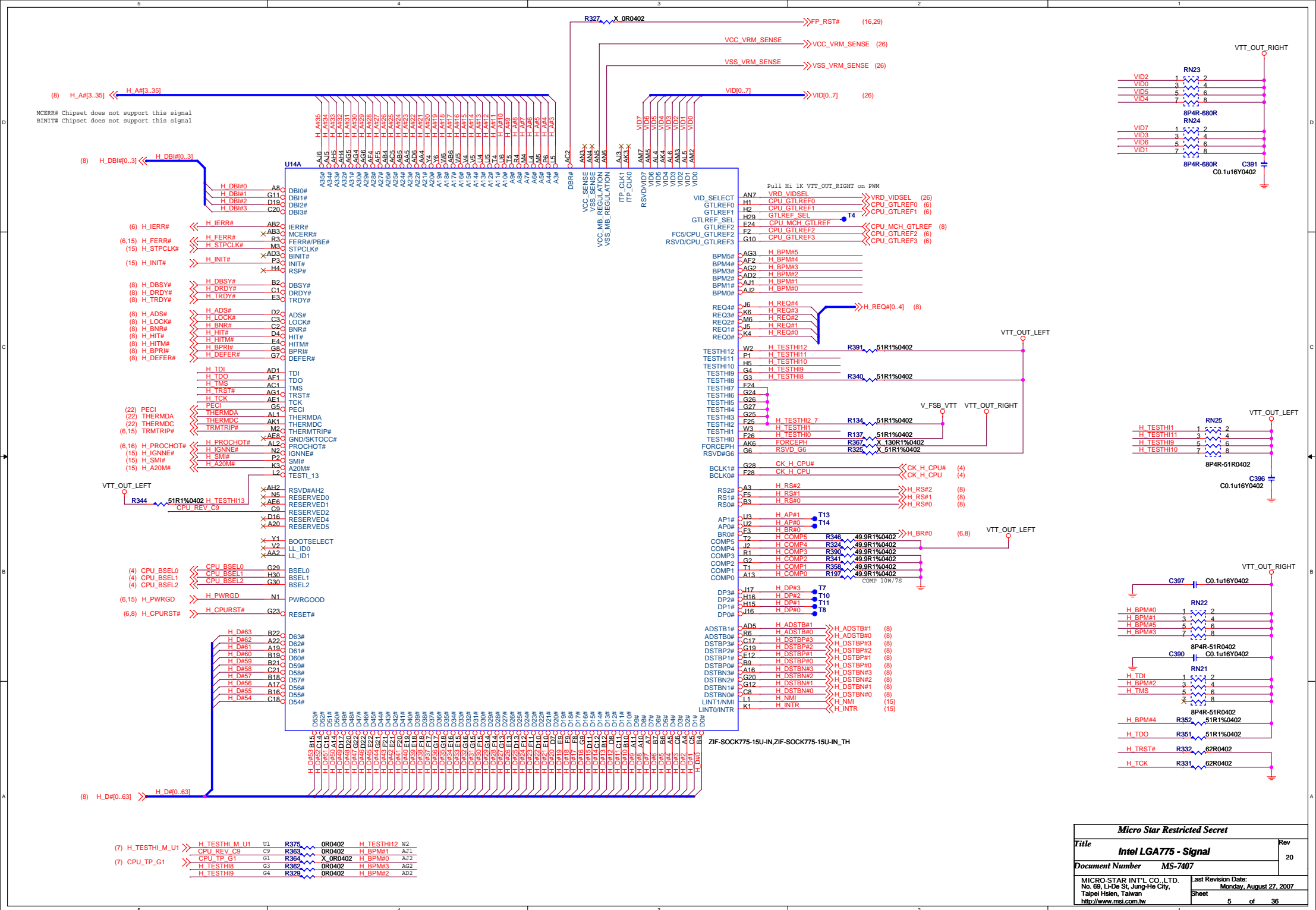
BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHz (1066)
0	1	0	200 MHz (800)
0	0	1	133 MHz (533)

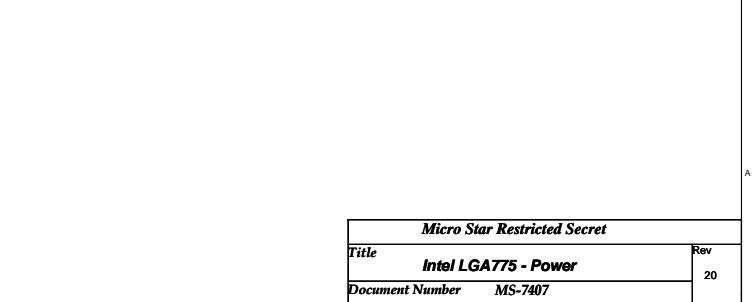
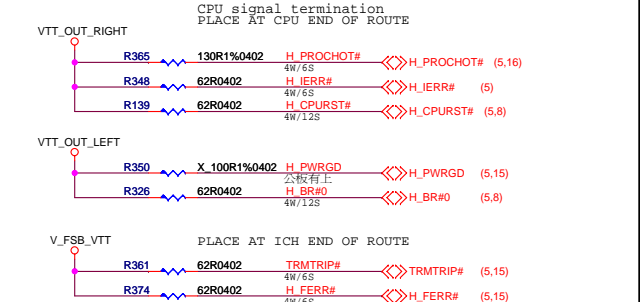
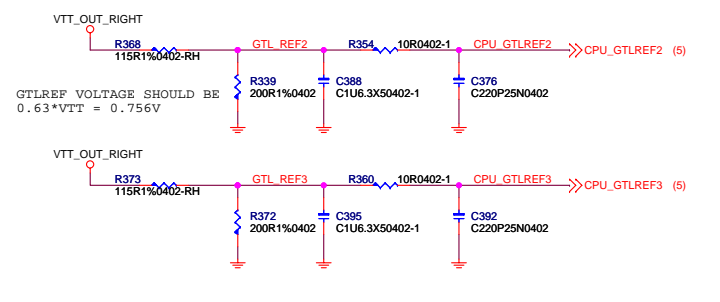
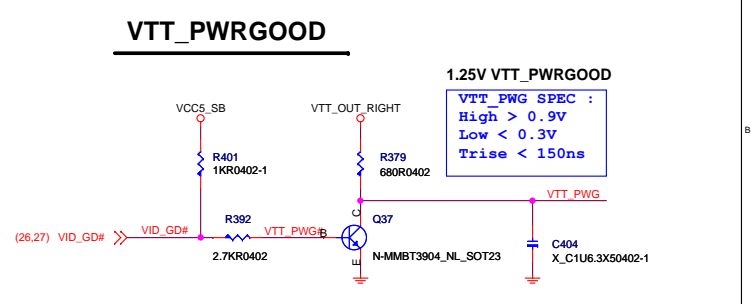
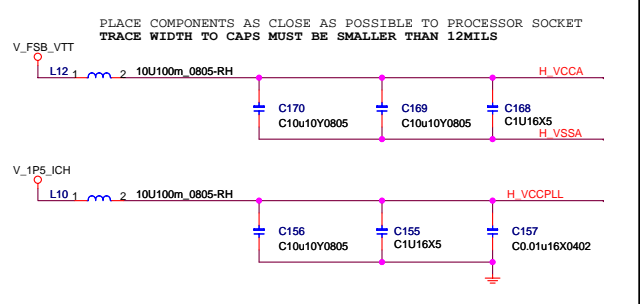
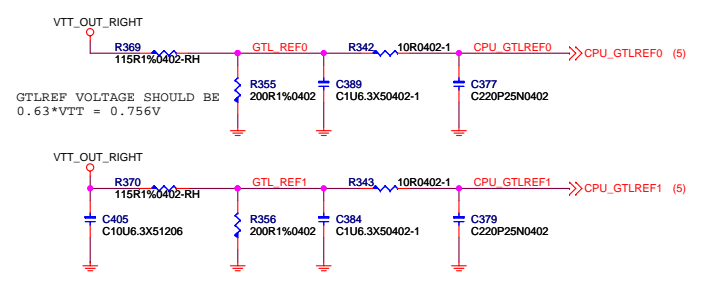
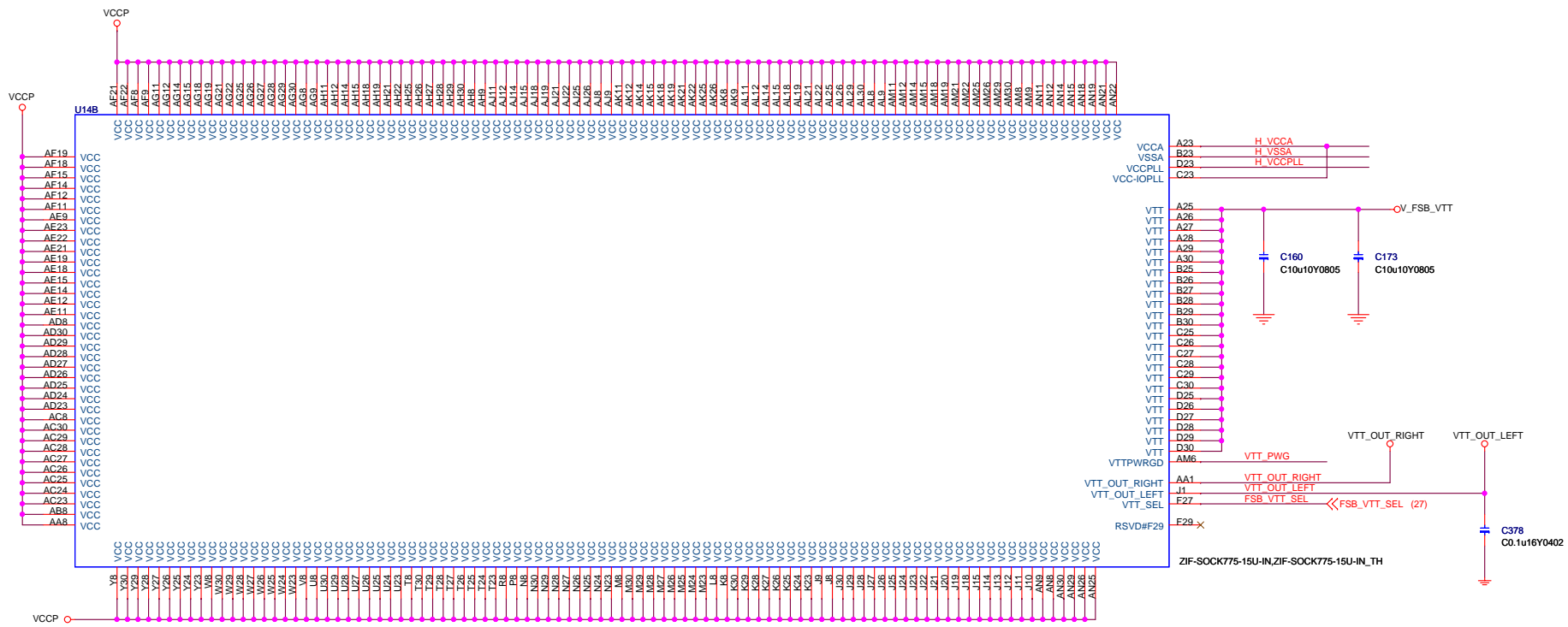
Trace length less than 0.5inches



SIGNAL	Pull-High	Pull-Low
SIOPCLK	Trusted Mode	Overclocking
SRC5_EN	Enable SRC5/SRC5#	Enable CPU_STOP#/PCI_STOP#
ITP_EN	CPU_ITPCLK	For SRCCLK8







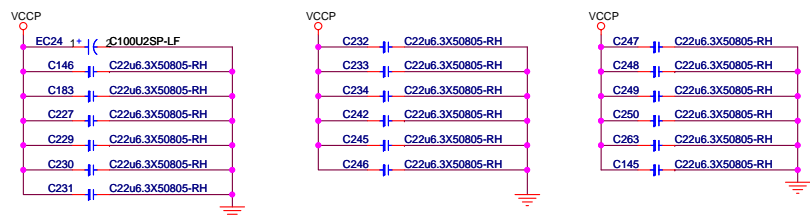
U14C

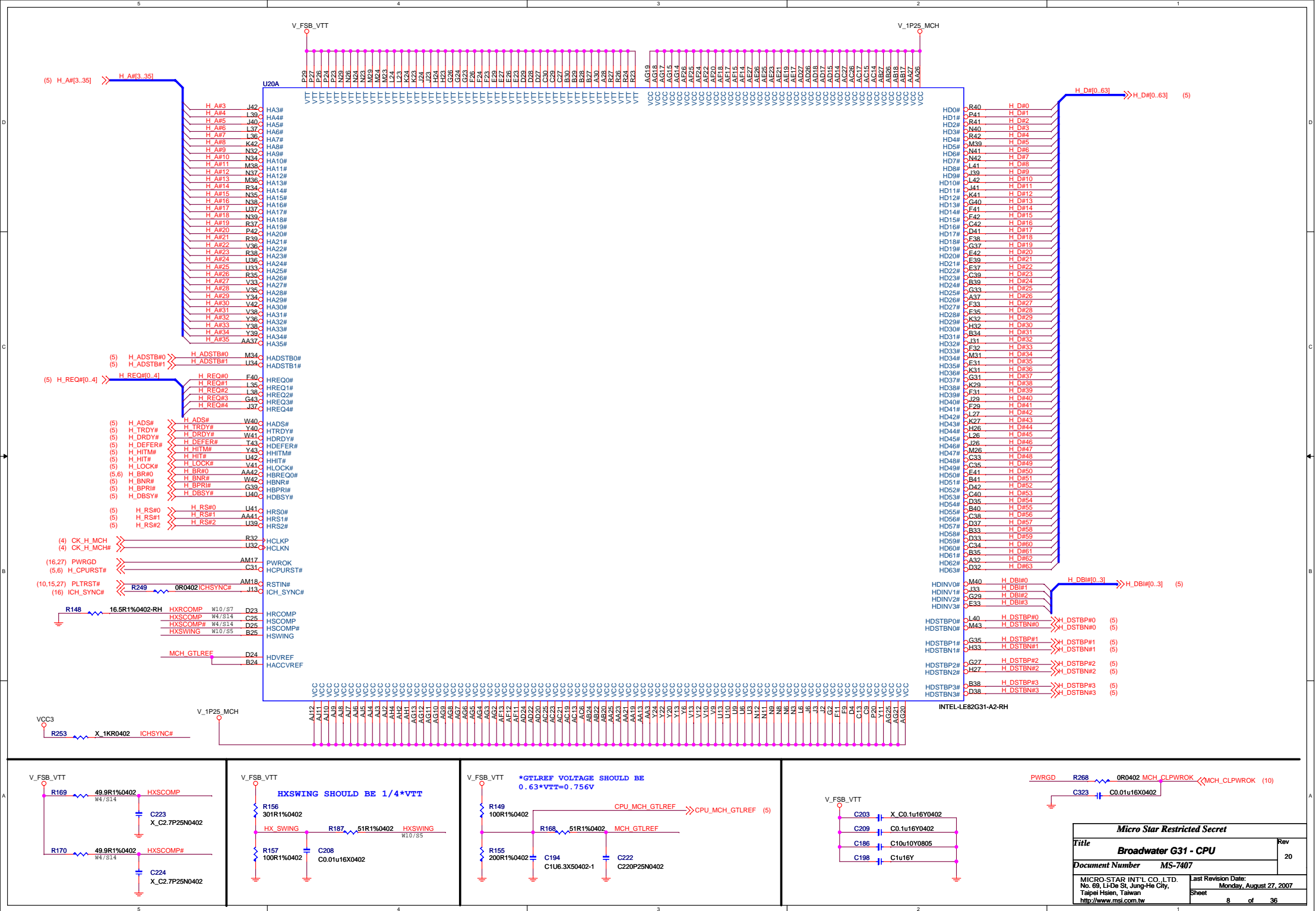
VTT_OUT_RIGHT

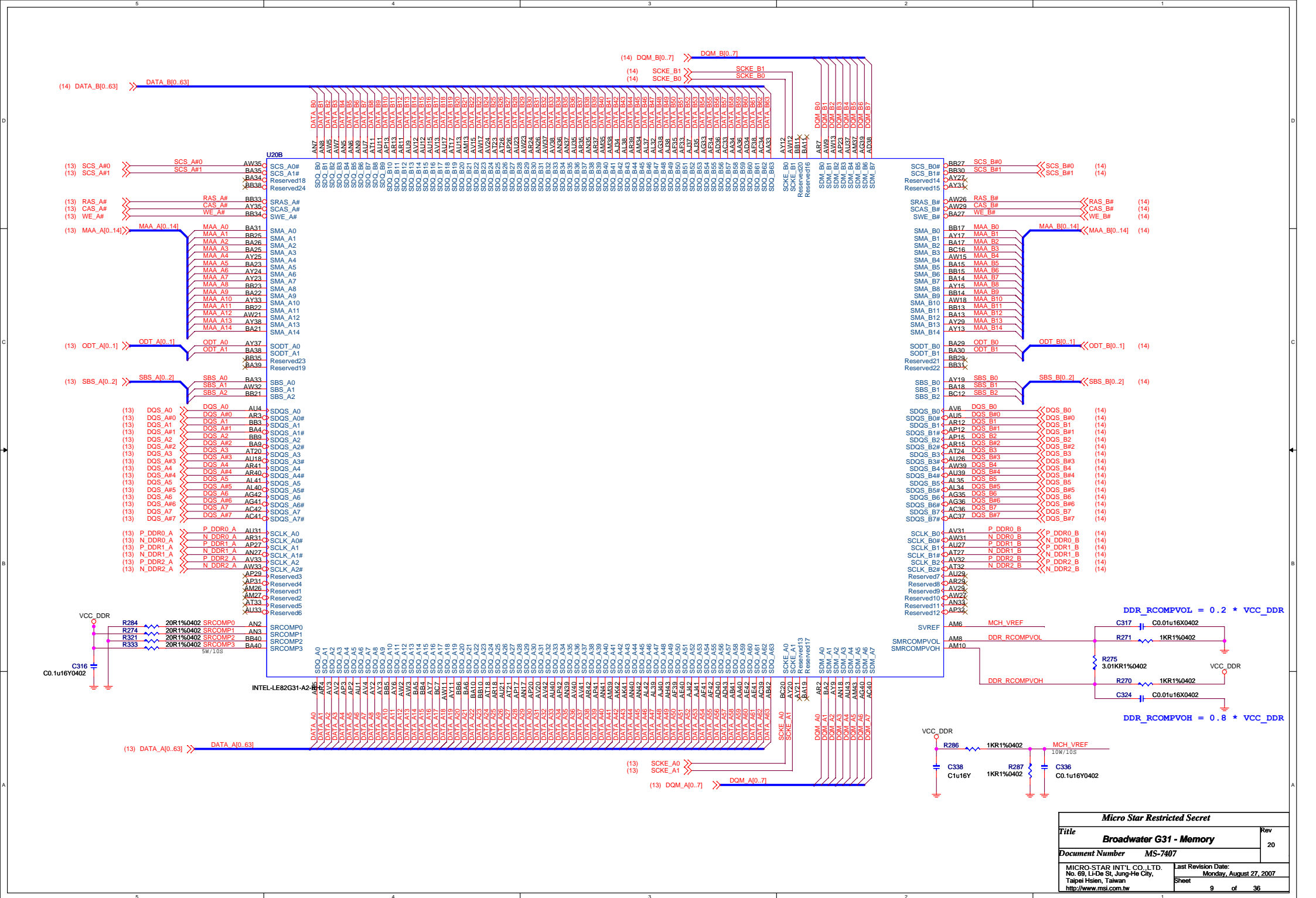
VTT_OUT_LEFT

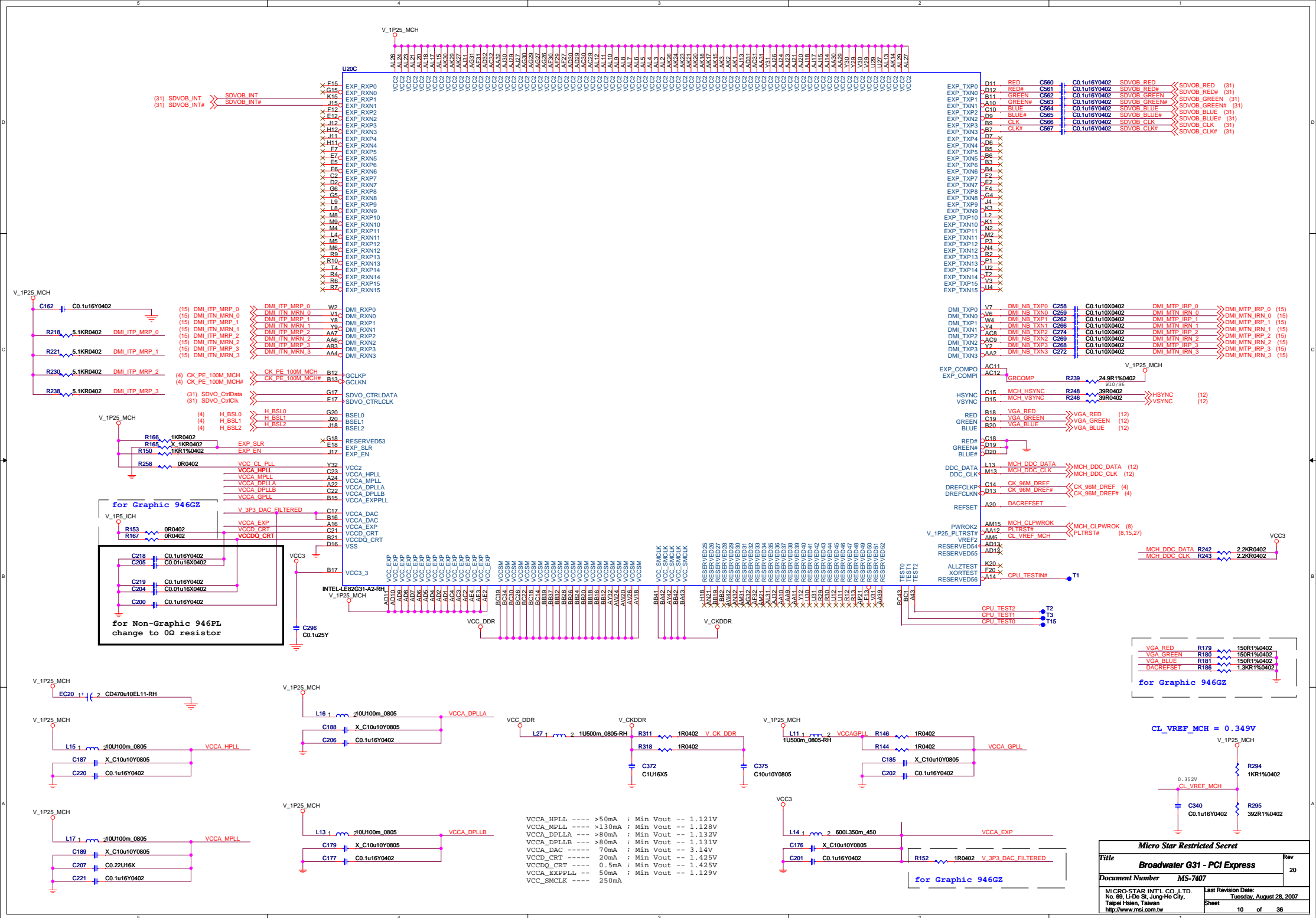
CPU_TP_G1
H_TESTHI_M_U1

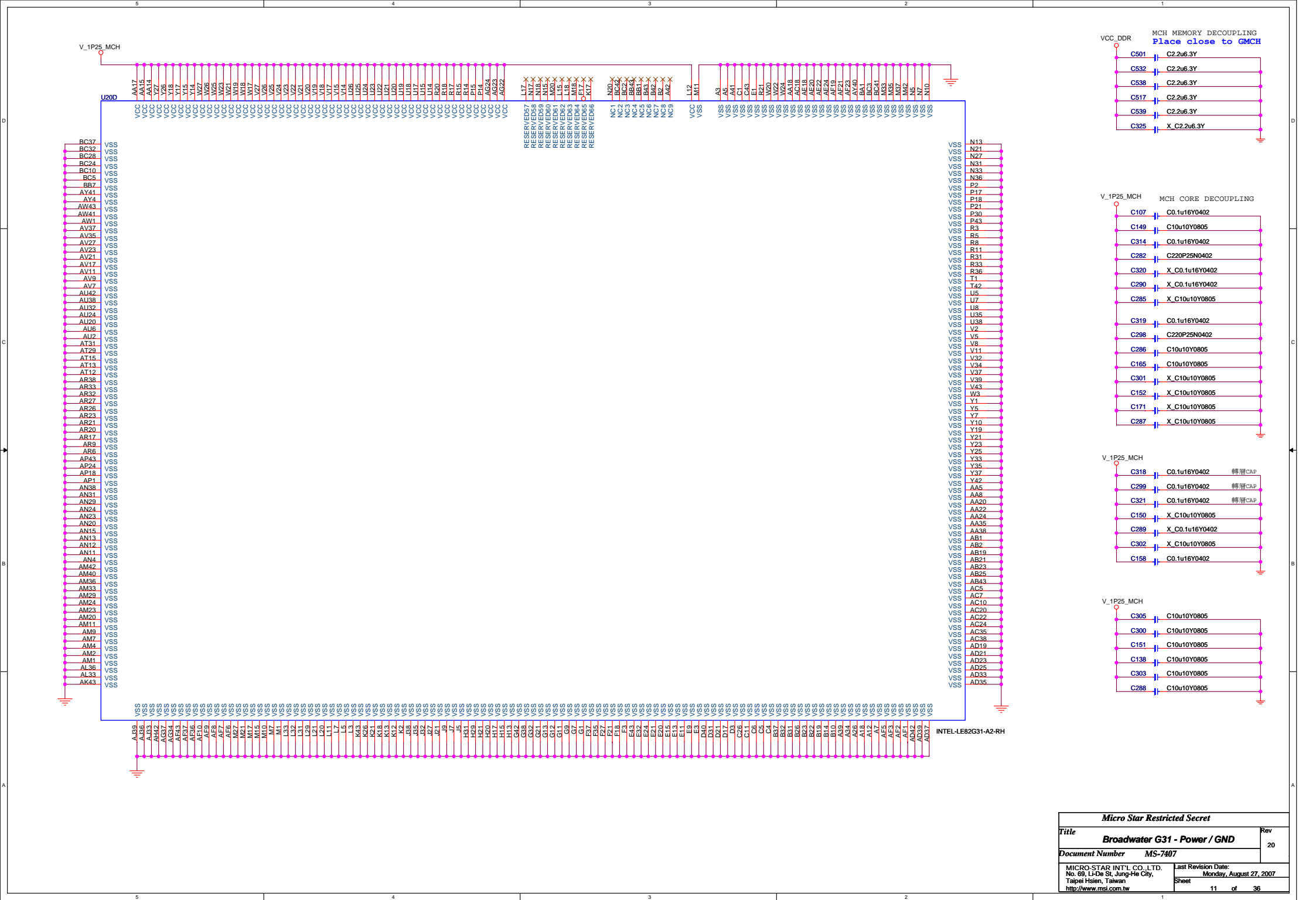
CPU DECOUPLING CAPACITORS



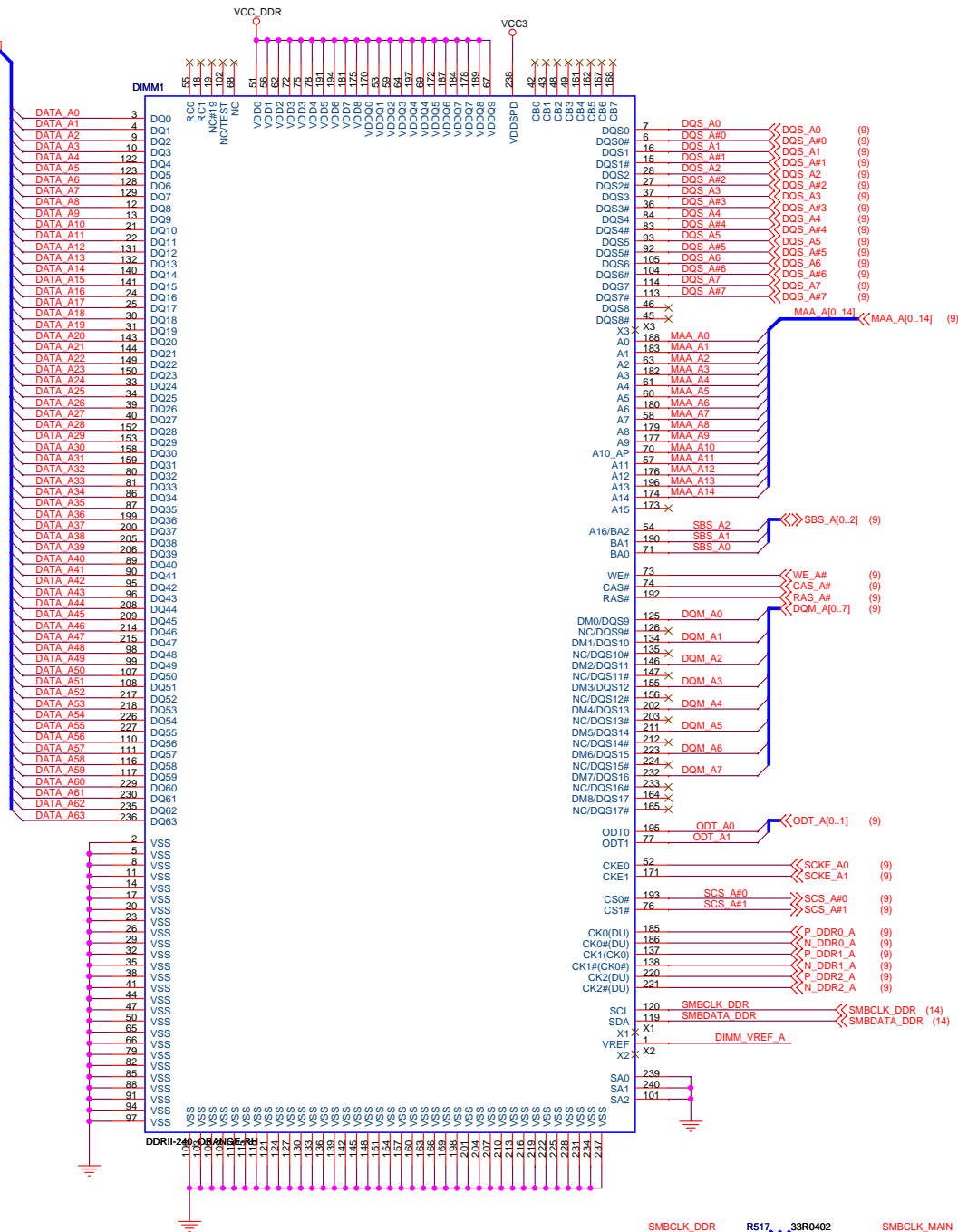




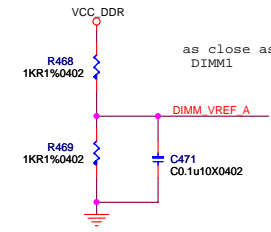




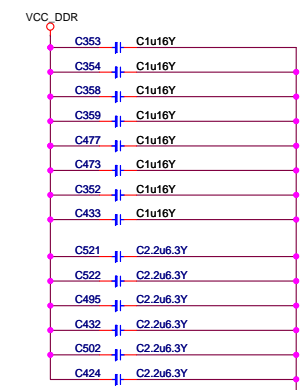
(9) DATA_A[0..63] <<> DATA_A[0..63]



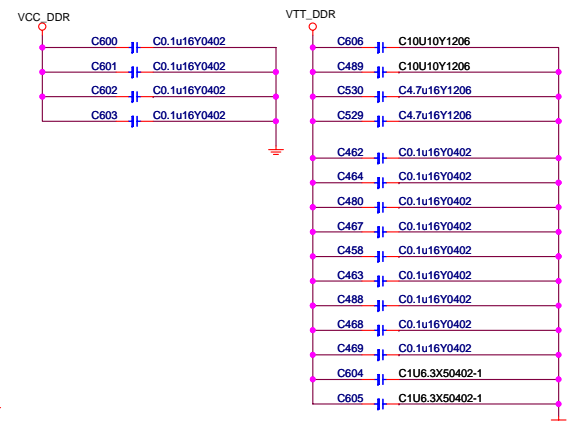
SMBCLK_DDR R517 33R0402 SMBCLK_MAIN <<> SMBCLK_MAIN (4,16,27)
SMBDATA_DDR R516 33R0402 SMBDATA_MAIN <<> SMBDATA_MAIN (4,16,27)



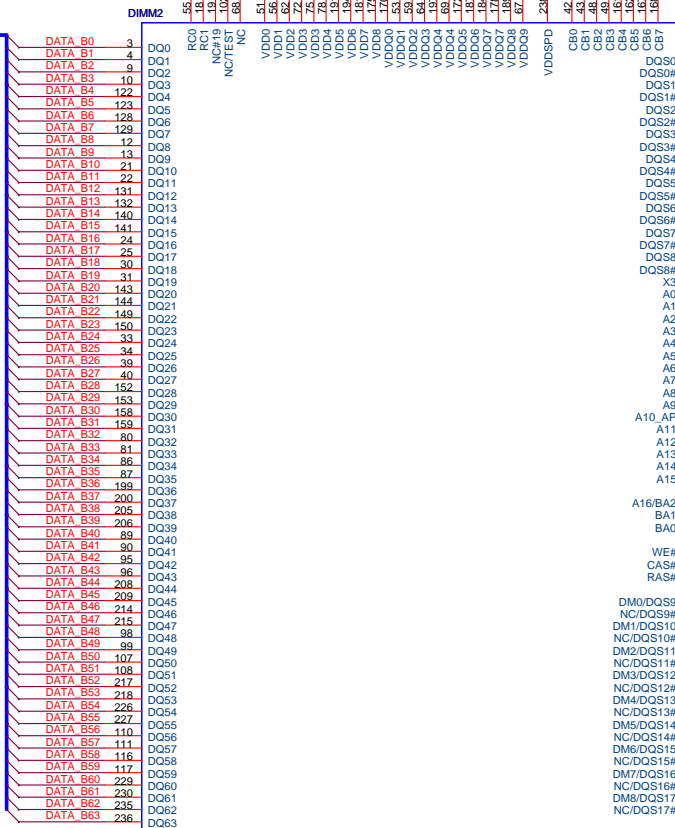
DIMM MEMORY DECOUPLING



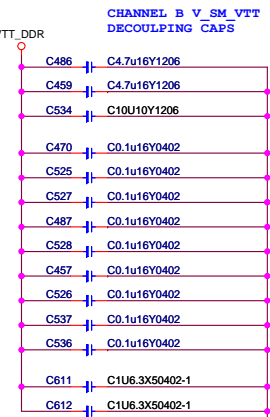
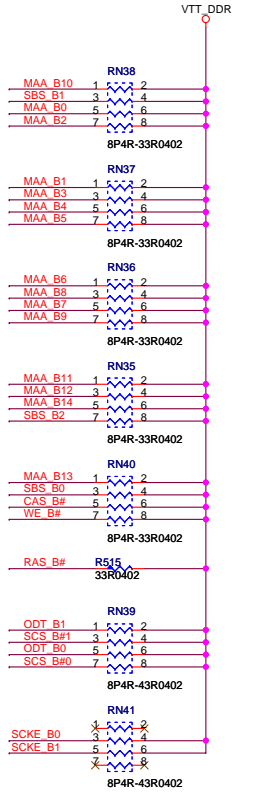
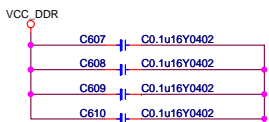
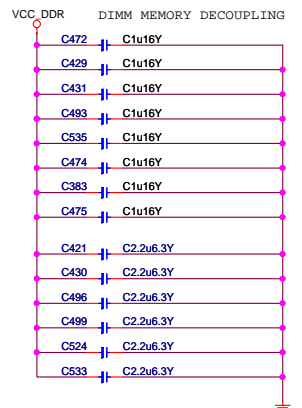
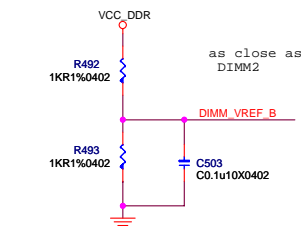
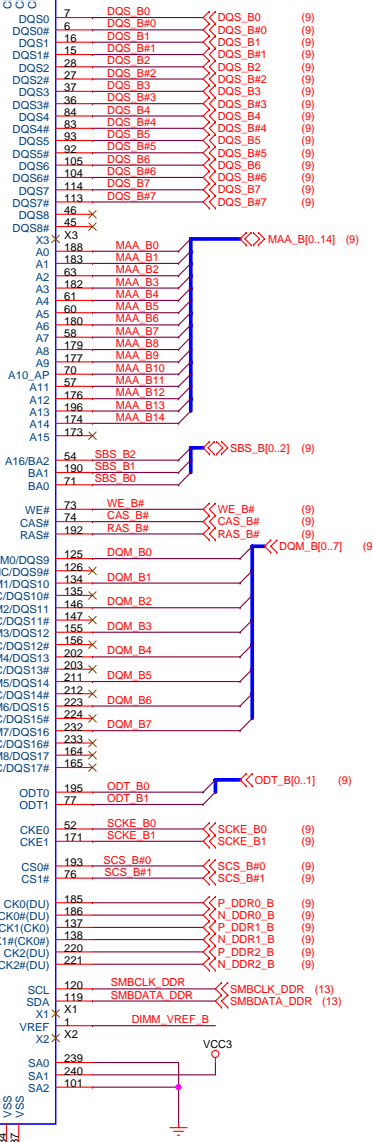
CHANNEL B V_SM VTT DECOUPLING CAPS



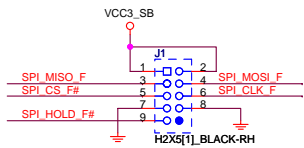
(9) DATA_B[0..63]



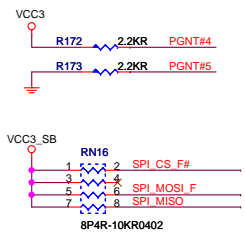
DDR1-240 OPEN B1



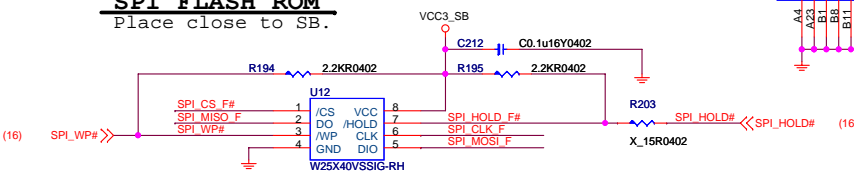
SPI DEBUG PROT Place close to SPI ROM



GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC

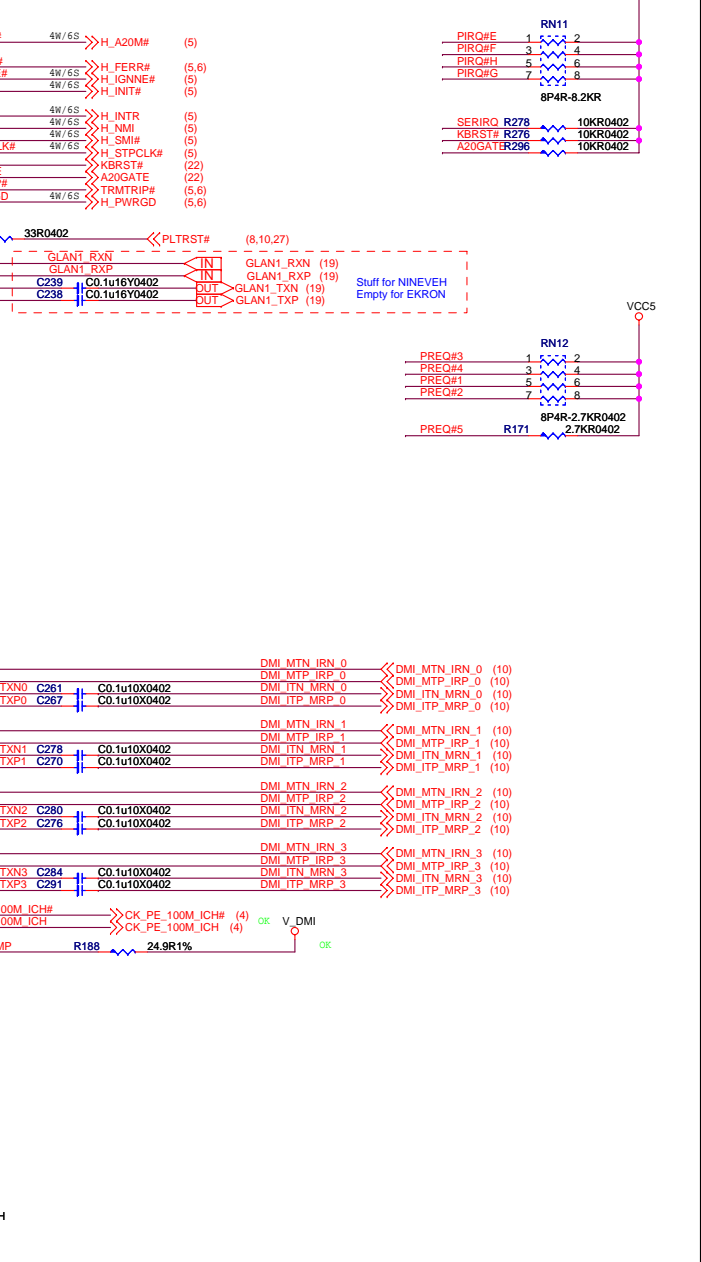
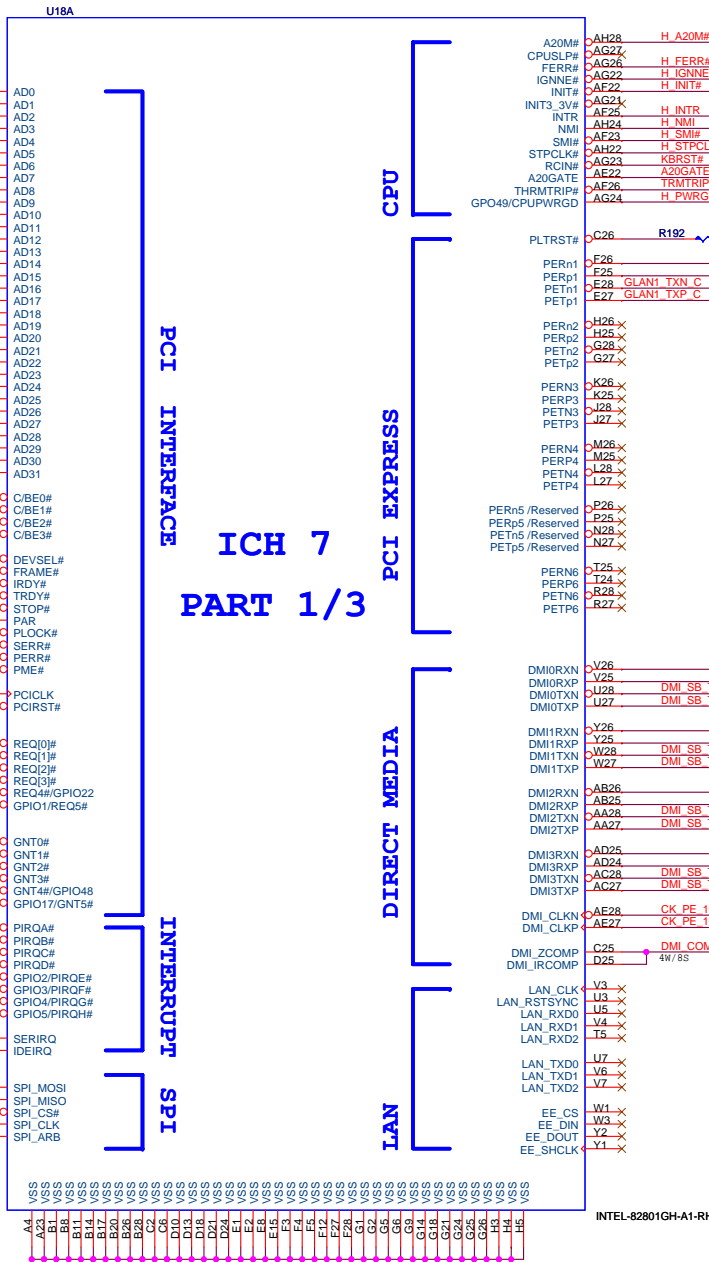


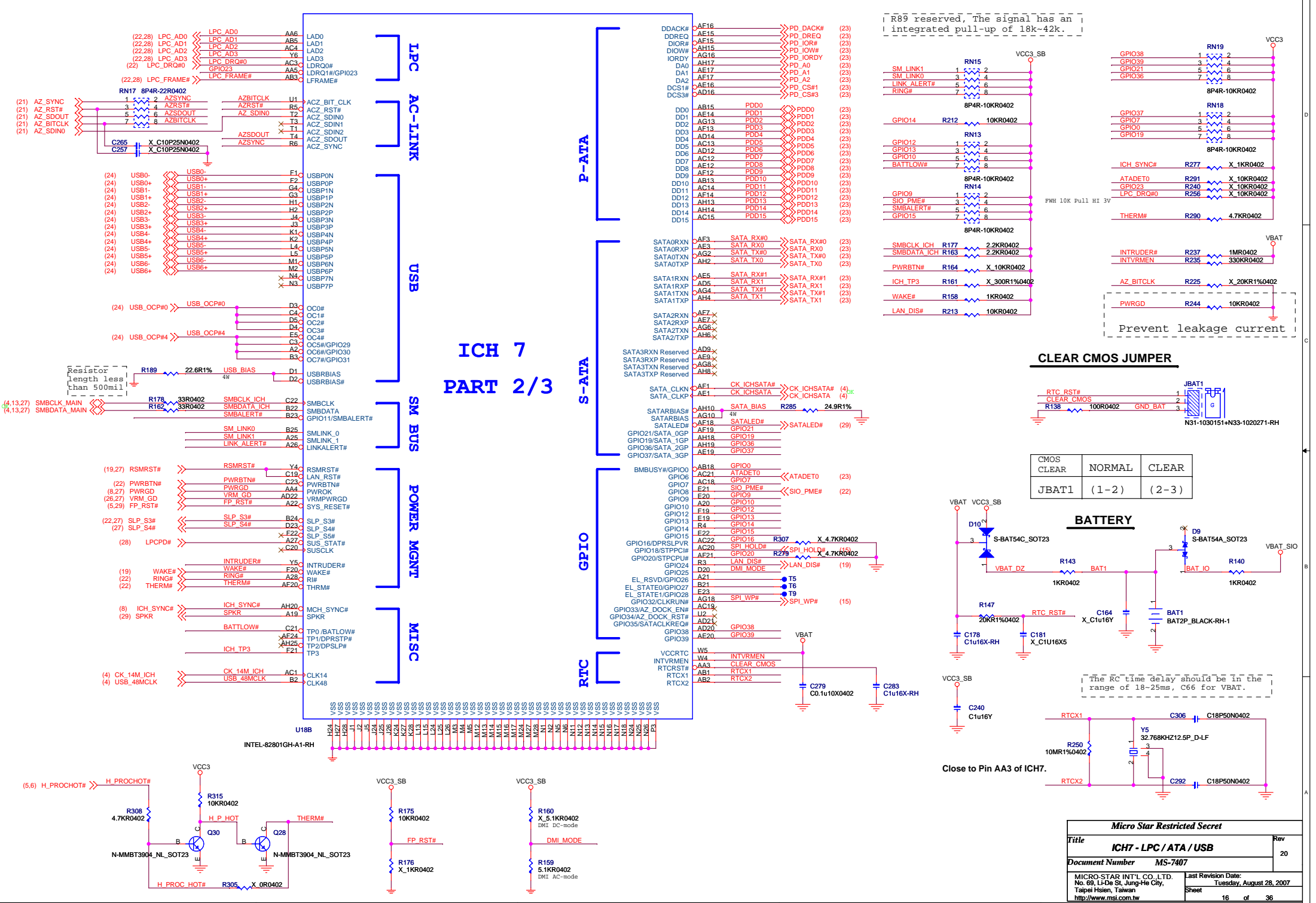
SPI FLASH ROM Place close to SB.



Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

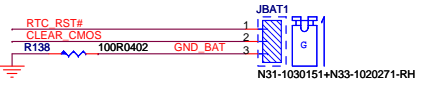
ICH 7 PART 1/3





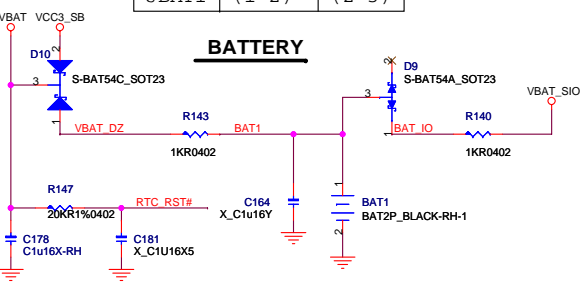
ICH 7
PART 2/3

CLEAR CMOS JUMPER

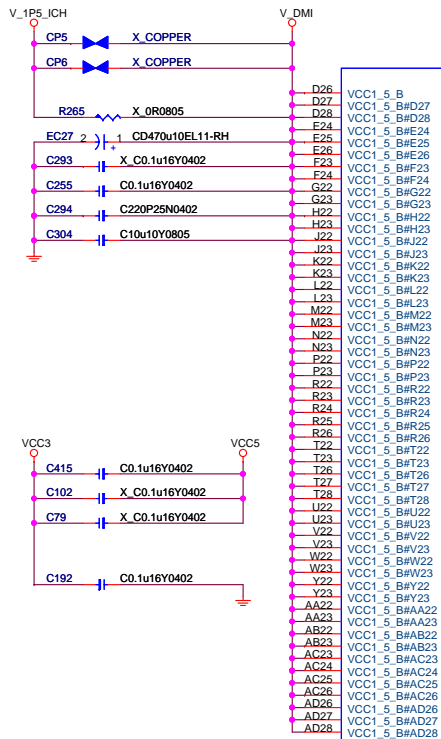


CMOS CLEAR	NORMAL	CLEAR
JBAT1	(1-2)	(2-3)

BATTERY



The RC time delay should be in the range of 18-25ms, C66 for VBAT.



1.5V DMI POWER

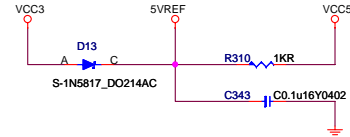
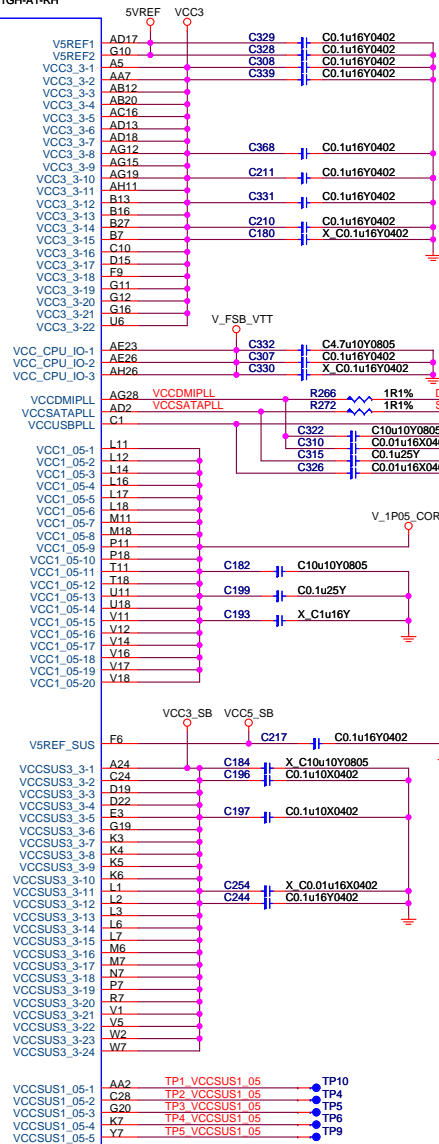
ICH 7 PART 3/3

1.5V CORE WELL POWER

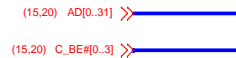


S0 POWER

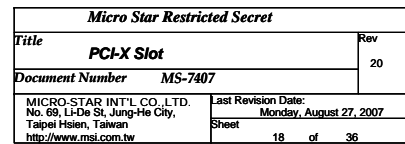
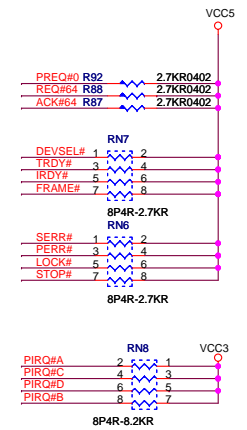
S5 POWER

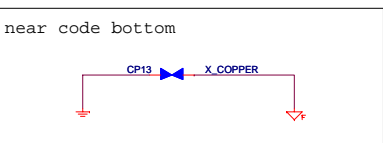
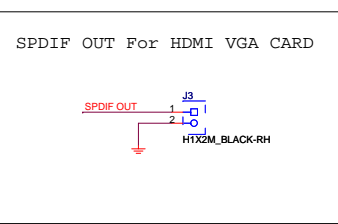
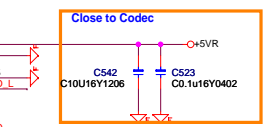
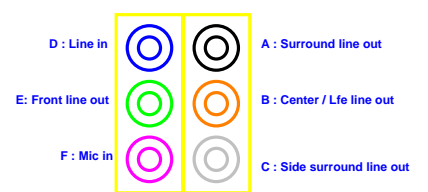
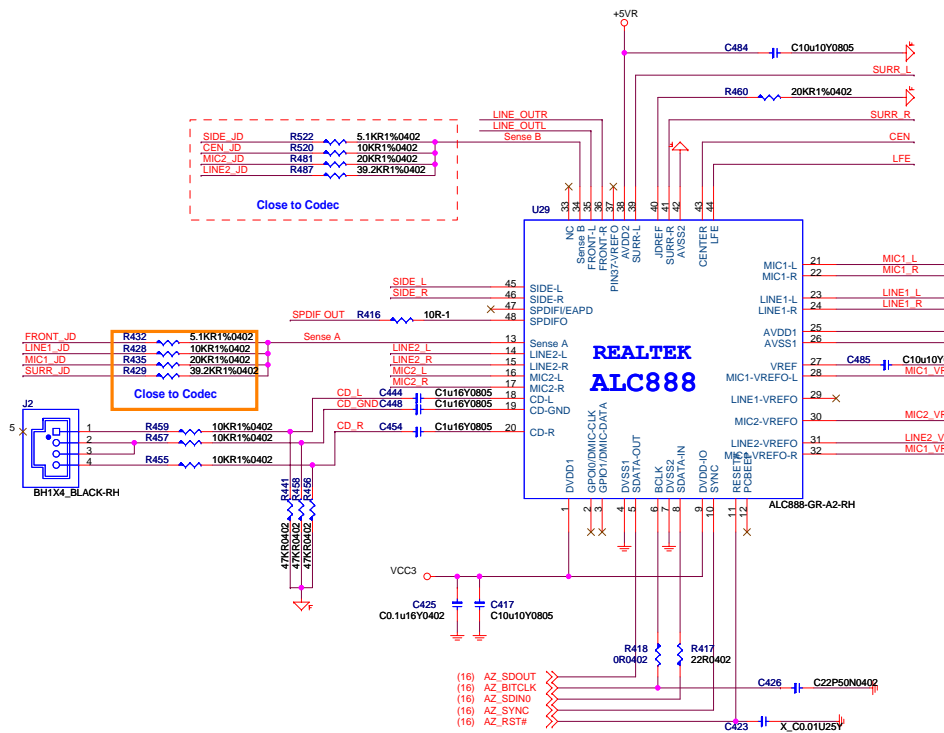


- VccDMIPLL --- 50mA
- VccUSBPLL --- 50mA
- VccSATAPLL --- 10mA
- VCC1_05 ----- 1.31A
- VCC1_5_A ----- 0.97mA
- VCC1_5_B ----- 0.74mA
- VCC3_3 ----- 0.58mA
- VCCSUS3_3 ----- 0.7A
- V5REF ----- 6mA
- V5REFSUS ----- 10mA
- V_CPU_IO ----- 14mA

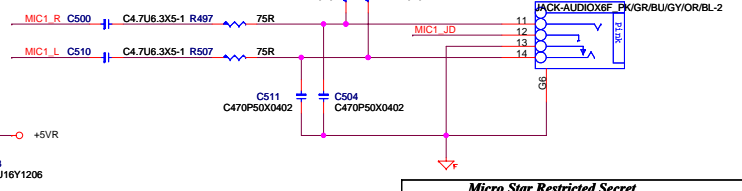
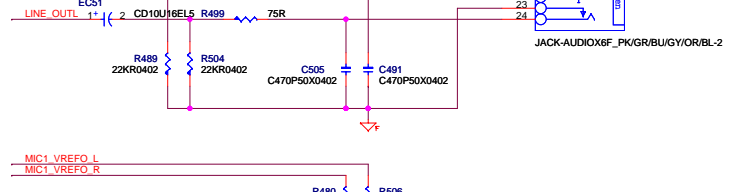
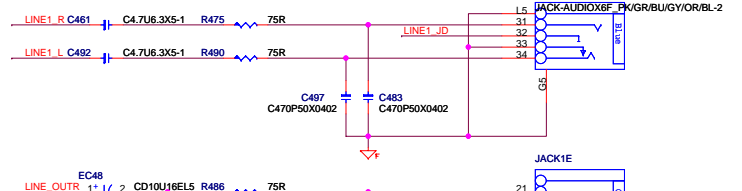
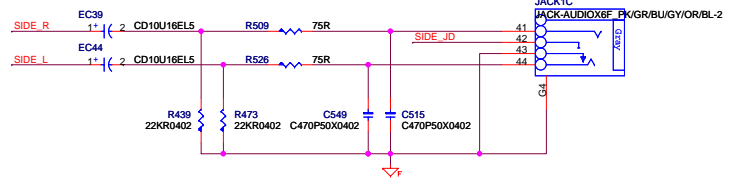
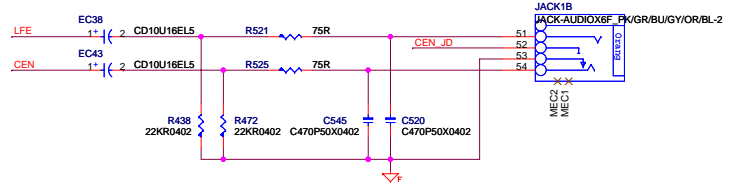
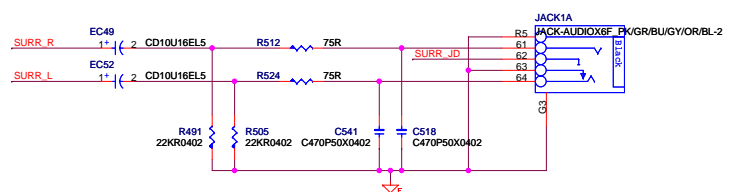
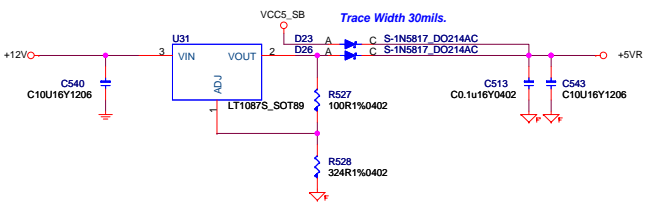


```
IDSEL: AD21
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REQ: PREQ#2
GNT: PGNT#2
CLK: PCI_CLK2
```

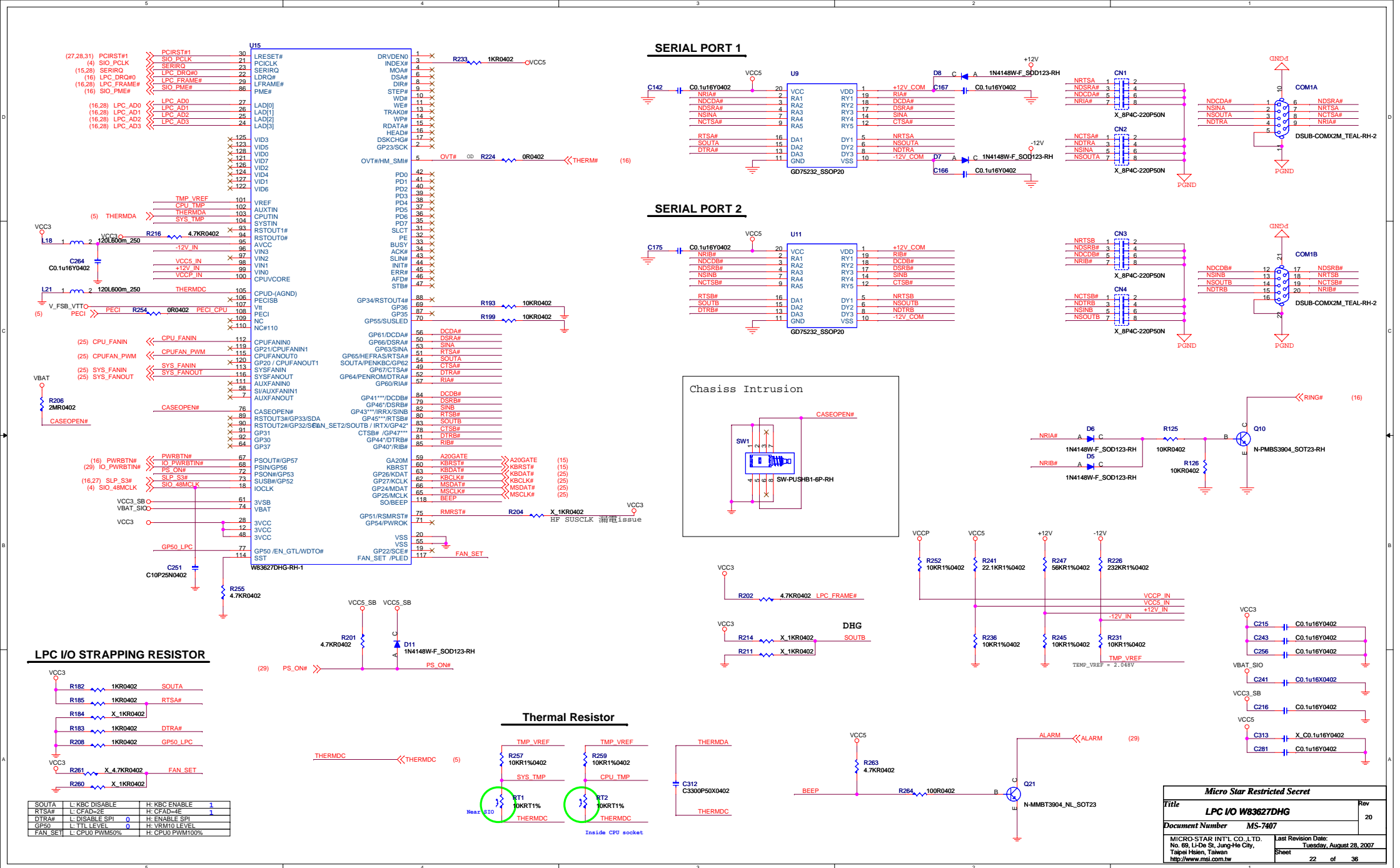




AUDIO CODE REGULATORS

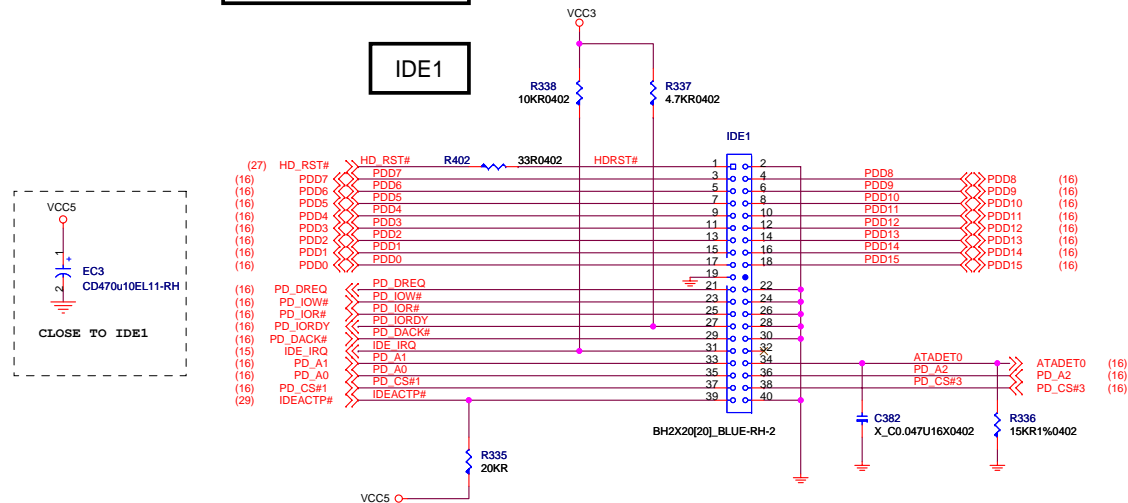


Micro Star Restricted Secret		
Title	Azalia CODEC ALC888	Rev 20
Document Number	MS-7407	
MICRO-STAR INT'L CO.,LTD. No. 68, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, August 28, 2007
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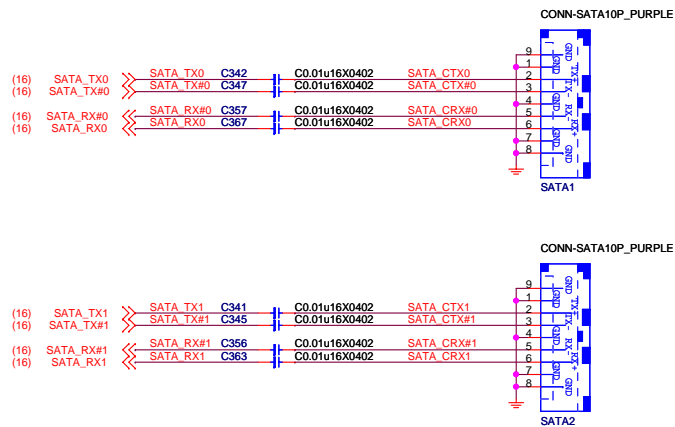


IDE Connector

IDE1



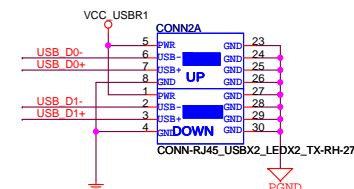
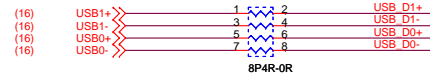
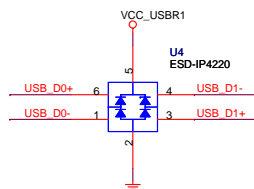
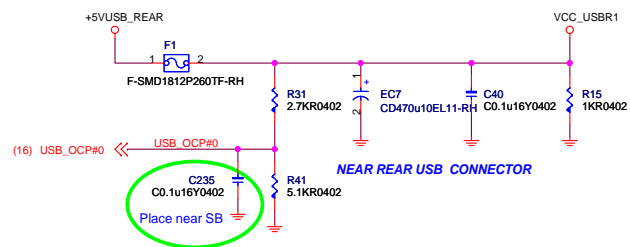
SATA CONNECTOR



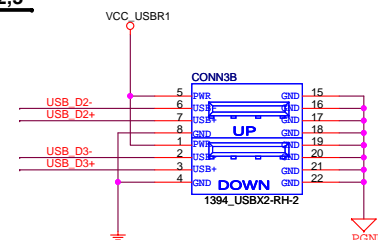
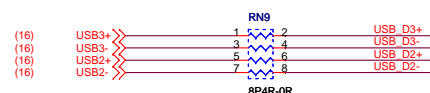
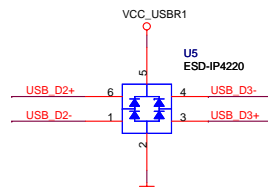
Micro Star Restricted Secret

Title		Rev
IDE /SATA Connector		20
Document Number		MS-7407
MICRO-STAR INT'L CO., LTD. No. 66, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, August 27, 2007 Sheet 23 of 36

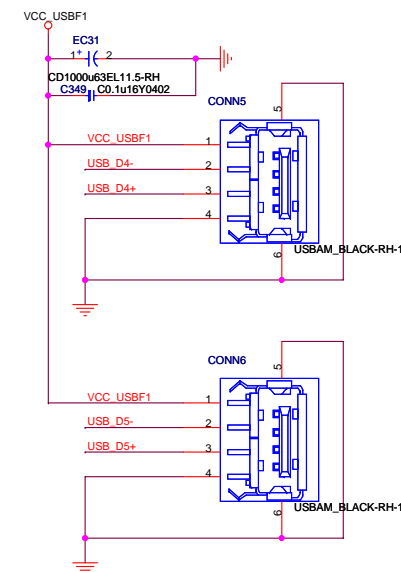
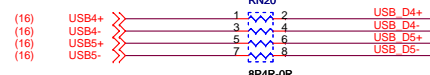
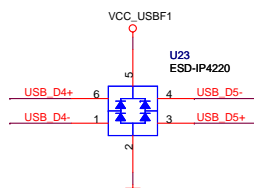
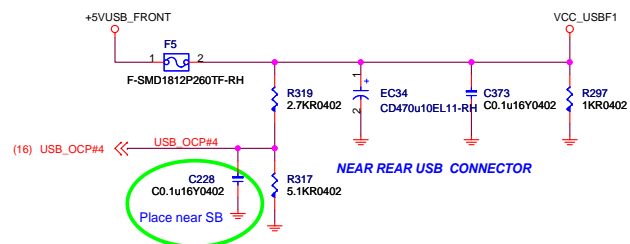
POWER CIRCUIT FOR USB PORT 0,1,2,3



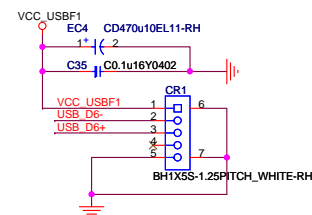
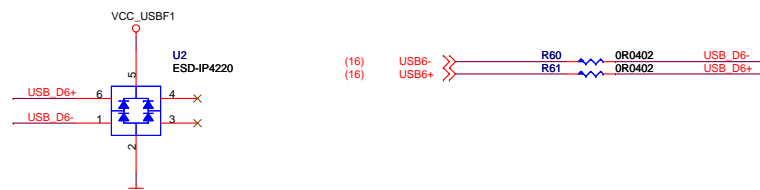
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 4,5



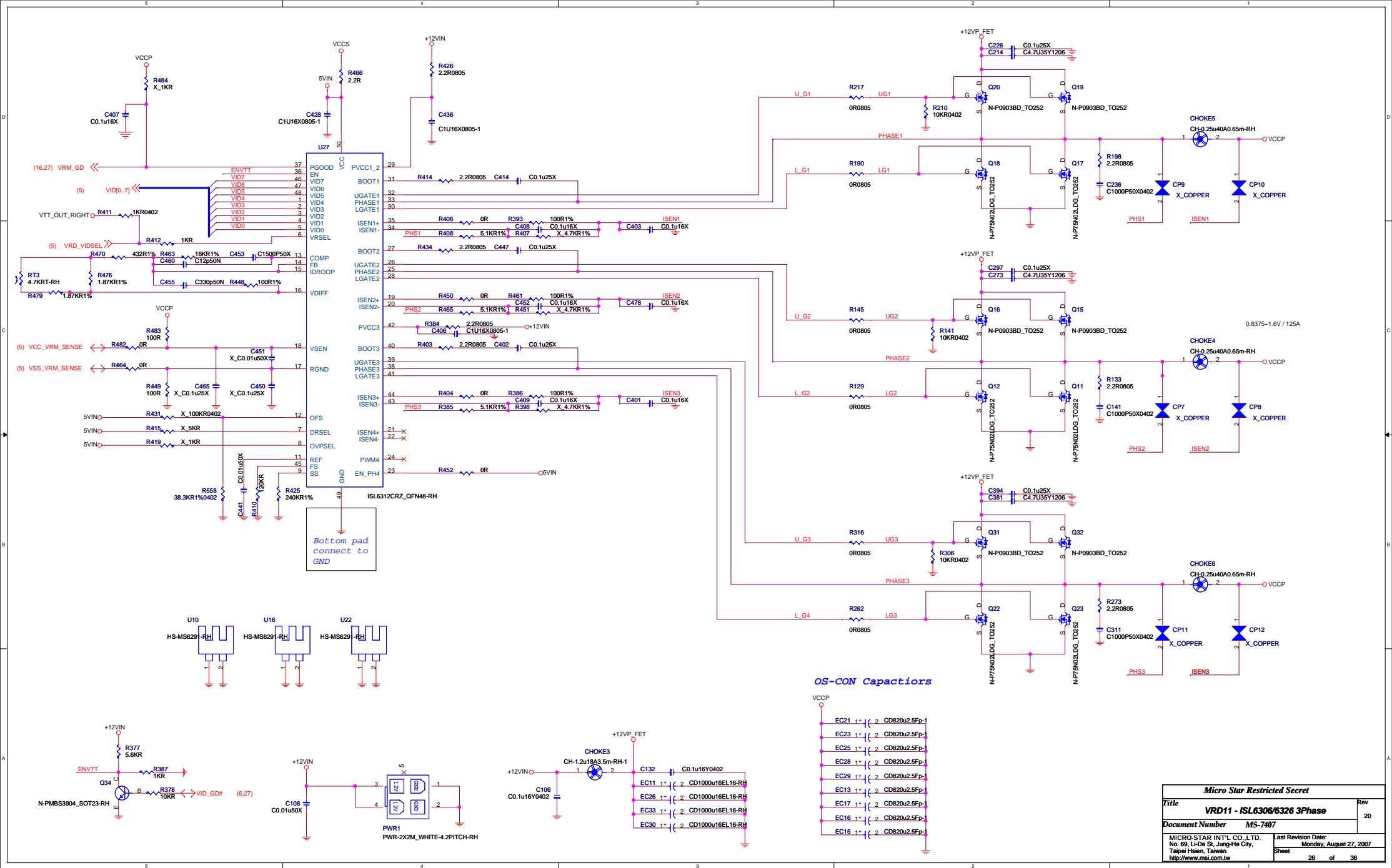
CARD READER USB CONNECTOR FOR USB PORT 6,



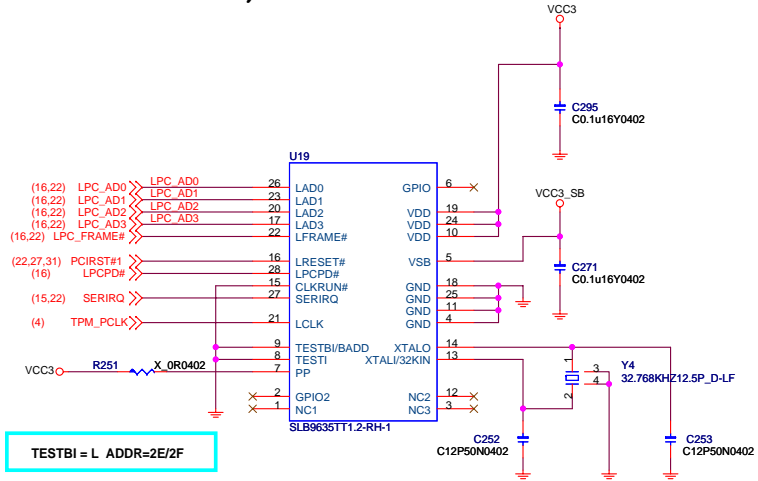
Micro Star Restricted Secret			
Title	USB Connector		Rev
Document Number	MS-7407		20
MICRO-STAR INT'L CO., LTD.		Last Revision Date:	
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http://www.msi.com.tw			

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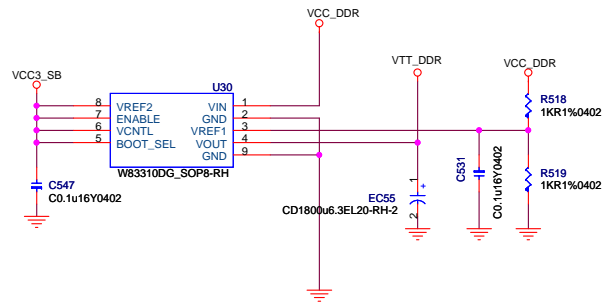
Micro Star Restricted Secret		
Title	KB/MS & FAN	Rev
Document Number	MS-7407	20
MICRO STAR INT'L CO. LTD. No. 69, L/D St, Jung-Hsie City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, August 27, 2007 <hr/> Sheet 25 of 36



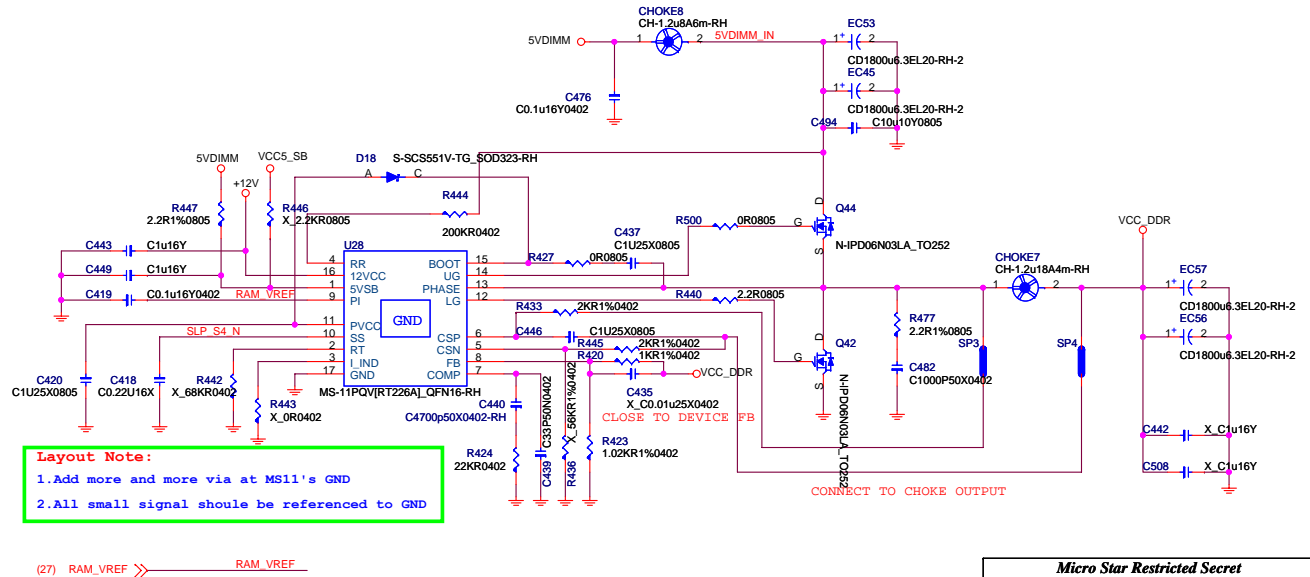
TPM - Security Controller



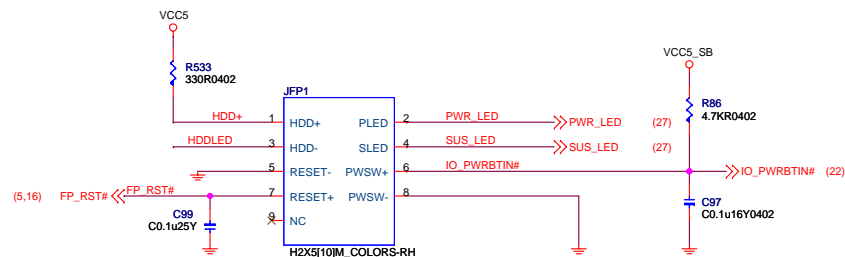
DDR II VTT POWER



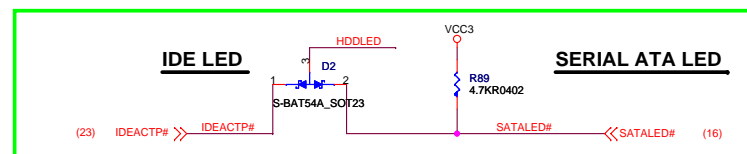
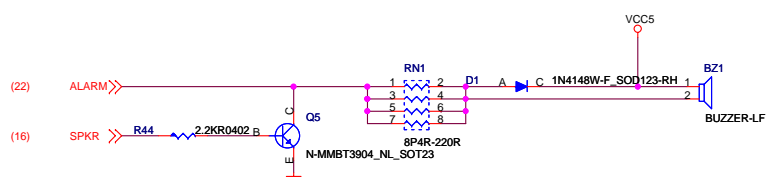
DDR II 1.8V POWER...16A



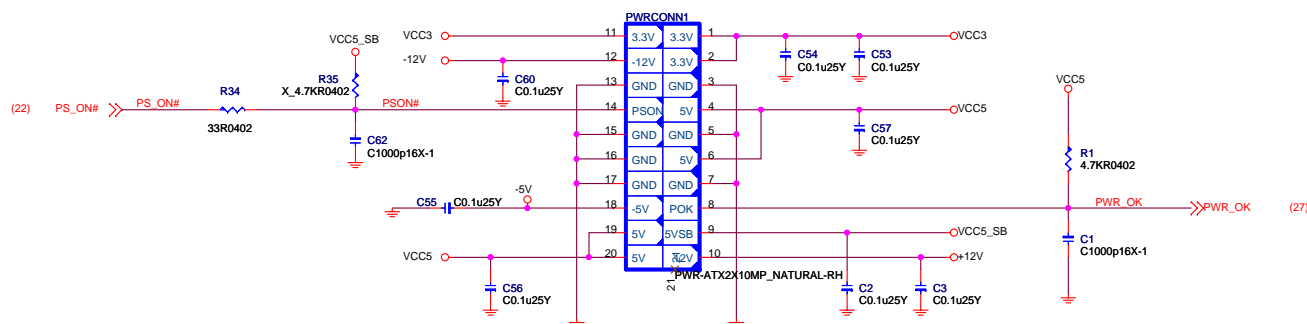
Intel Front Panel



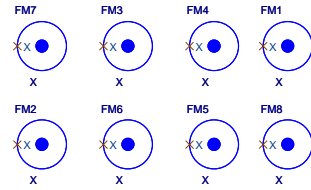
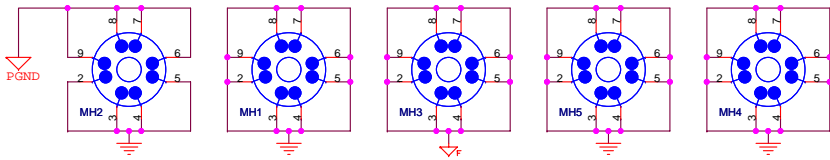
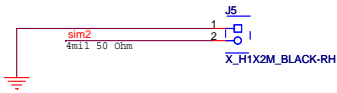
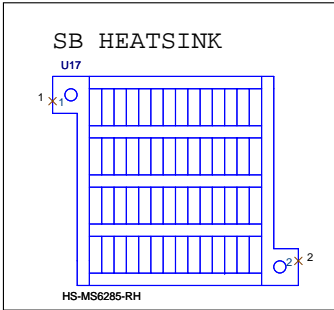
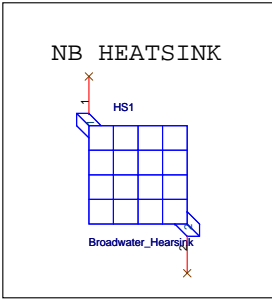
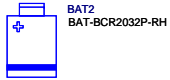
BUZZER



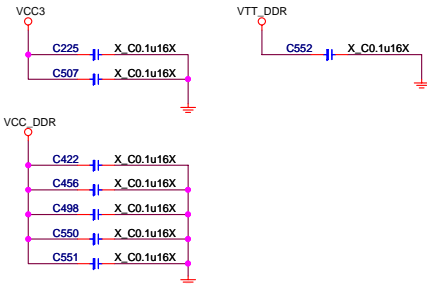
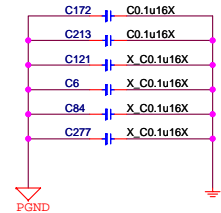
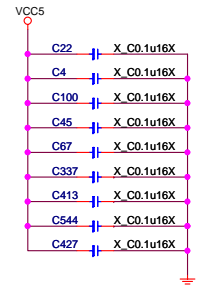
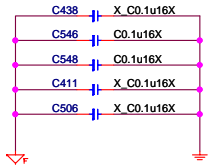
ATX



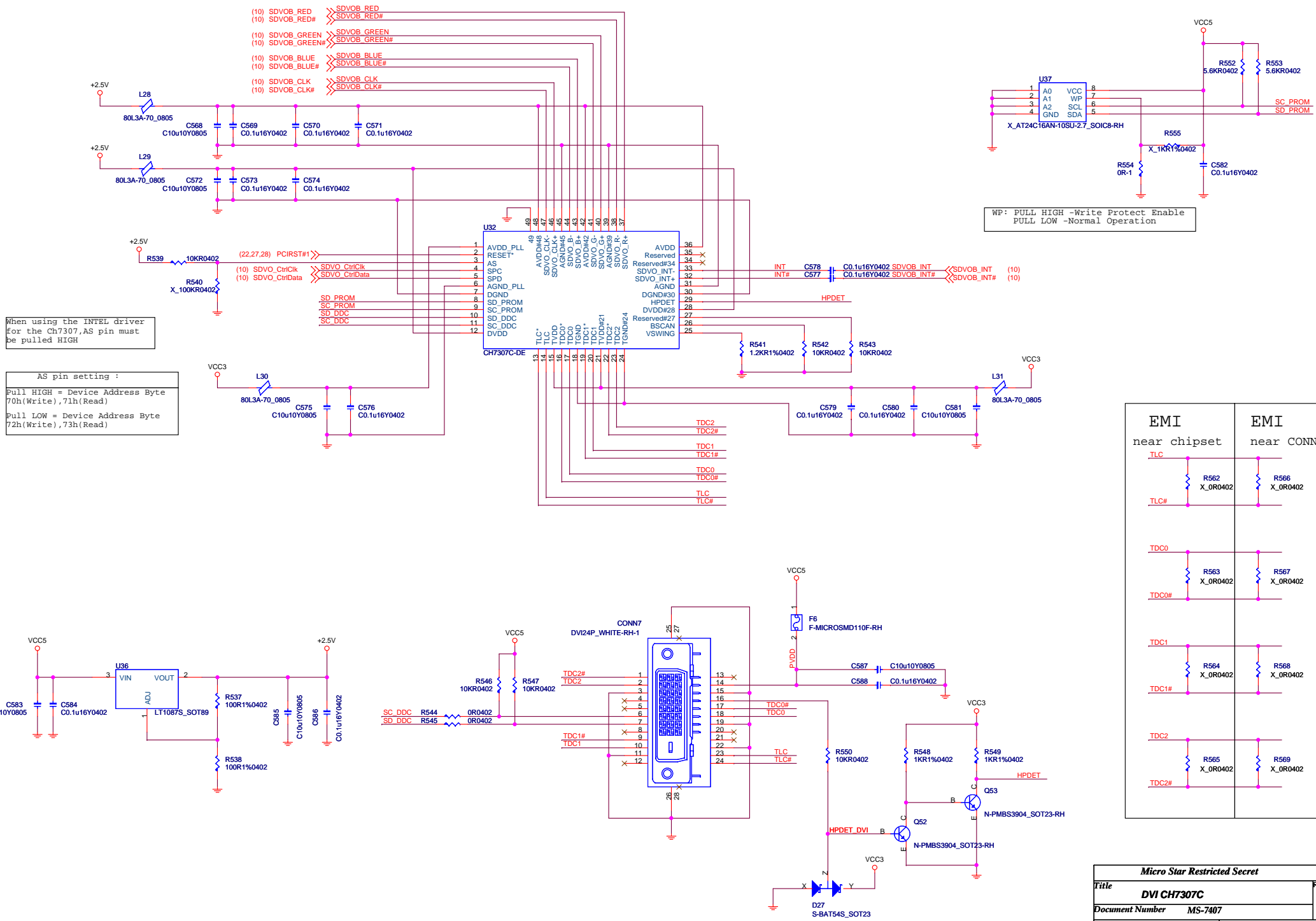
Micro Star Restricted Secret		
Title	Front ATX & Panel & LED	Rev 20
Document Number	MS-7407	
MICRO-STAR INT'L CO., LTD. No. 66, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, August 27, 2007 Sheet 29 of 36



EMI



Micro Star Restricted Secret		
Title	Manual Parts	Rev 20
Document Number	MS-7407	
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MS-7407 bug history list					
1	Remove R128 for 1394 EEPROM	6/27	31		
2	Change Lan chipset to 82573L	6/27	32		
3	Add Q50 and EC58 for VCC3_SB	6/27	33		
4	Change U12 SPI ROM 16M to 8M	7/5	34		
5	Change Y4 to DIP D04-0300121-K11(TPM)	7/20	35		
6	Add CP13 for AGND link GND(Audio)	7/20	36		
7	Change L24,L25,L26 to L01-82CA013-T34(VGA)	7/20	37		
8	Change C344,C348,C355,C366,C369,C371 to C11-33A1812-W08(VGA)	7/20	38		
9	Modify C123 to C11-1032082-W08 10000 pf (Power team)	7/20	39		
10	Modify R104 to R11-0103T12-W08 10Kohm 1% (Power team)	7/20	40		
11	Modify R190,R129,R262 to 0 ohm 1% (Power team)	7/20	41		
12	Modify C440 to C11-4722812-T34 4700pf (Power team)	7/20	42		
13	Add R558 to 38.3K ohm (Power team)	7/20	43		
14	Modify VRM_GD link Circuit between ICH7 and MS-7, Remove R298,install R353	7/20	44		
15	Modify CK_PWRGD Circuit,add Q51,R557,C553	7/20	45		
16	Add R559 link 1P2VREF to GND (Power team)	7/20			
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Micro Star Restricted Secret

Title

Revision History

Document Number

MS-7407

MICRO-STAR INT'L CO.,LTD.
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MS-7407 bug history list					
1	Remove R128 for 1394 EEPROM	6/27	31		
2	Change Lan chipset to 82573L	6/27	32		
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Title

Revision History

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MS-7407 bug history list					
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LGA775 - CPU (65W)		
0.850V-1.3525V Core	-	125A
1.2V FSB VTT	-	5.3A

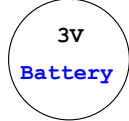
G31		
1.2V FSB_VTT	-	1.0A
1.25V Core	-	18.1A
1.25V DMI/PCI Exp.	-	2.5 A
1.8V VCC_DDR (S0,S1)	-	3.2A
1.8V VCC_SMCLK	-	250mA
3.3V VCCA_DAC	-	65.8mA
3.3V VCC33	-	15.8mA
1.25V Vcc CL	-	3.8A

ICH7		
1.05V Core	-	1.31A
1.5V DMI	-	40 mA
1.2V FSB_VTT	-	14 mA
1.5V_A USB/SATA	-	0.97A
1.5V_B PCI Exp.	-	0.74A
VCCRTC	-	6 uA
3.3V CL	-	12 mA
1.5V GbE LAN	-	74 mA
3.3V 10/100 LAN	-	12 mA
3.3V GbE LAN	-	1 mA
3.3V SusHDA	-	4 mA
3.3V HDA	-	24 mA
3.3V VccSus3_3	-	700mA
3.3V Vcc3_3	-	580mA

HD Audio ALC888		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

ICS9LP505		
3.3V VDD_48/PCI/REF	-	TBDA

INTEL 82566DC		
3.3V_SB I/O & LED	-	28mA
1.8V ANALOG	-	440mA
1.0V ANALOG	-	297mA



ISL6312		
VCCP	VRM 11	
0.850V-1.3525V		
3-Phase Switch	125A	

W83310DS		
VTT_DDR		
0.9V Linear	1.2A	

MS11+ Regulator		
VCC_DDR		
1.8V PWM		
4.7A+4.1A+2.5A	12A	

MS11+ Regulator		
V_1P25_MCH		
1.25V PWM		
20.6A+6A	26.6A	

MS7 Regulator		
V_1P25_CL		
V_FSB_VTT		
1.2V Linear	6.3A	
V_1P5_ICH		
1.5V Linear	2A+1A	
V_1P05_ICH		
1.05V Linear	1.31A	
5V DUAL		
5V Switch	4A	
5VSB Switch	500mA	
5VDIMM		
5V Switch	6.2A	
5VSB Switch	500mA	

5VAUD		
5V		
500mA		

1.8V	440mA
1.0V	297mA

VCC5_SB	VCC5	VCC3_SB	VCC3	+12V
Switch	21.5A	Switch	8.4A	Switch
1A		1.5A		9.5A
ATX POWER CONN				

DDRII x2 & TERMINATOR		
0.9V VTT_DDR	-	1.2A
1.8V VCC_DDR (S0,S1)	-	4.7A
1.8V VCC_DDR (S3)	-	400mA

PCI Express x16 slot		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

PCI slot x1		
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	7.6A
+5V	-	5.0A
+12V	-	0.5A

USB x7		
+5V (S0,S1)	-	3.5A
+5V (S3)	-	17.5mA

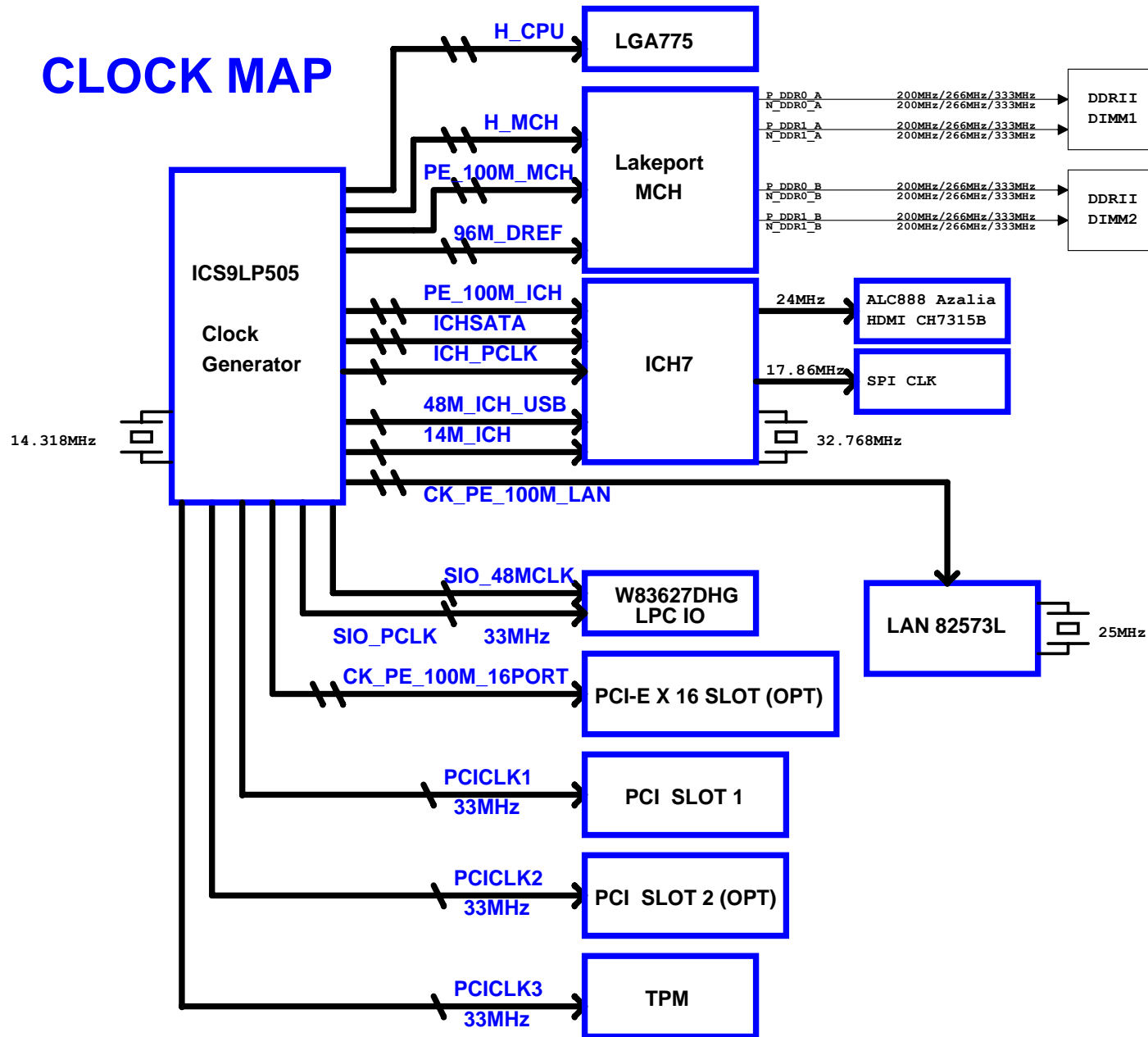
+12V CPU & SYS FAN		
	-	0.5A

DC 4Pin Output		
+12V		
+5V		

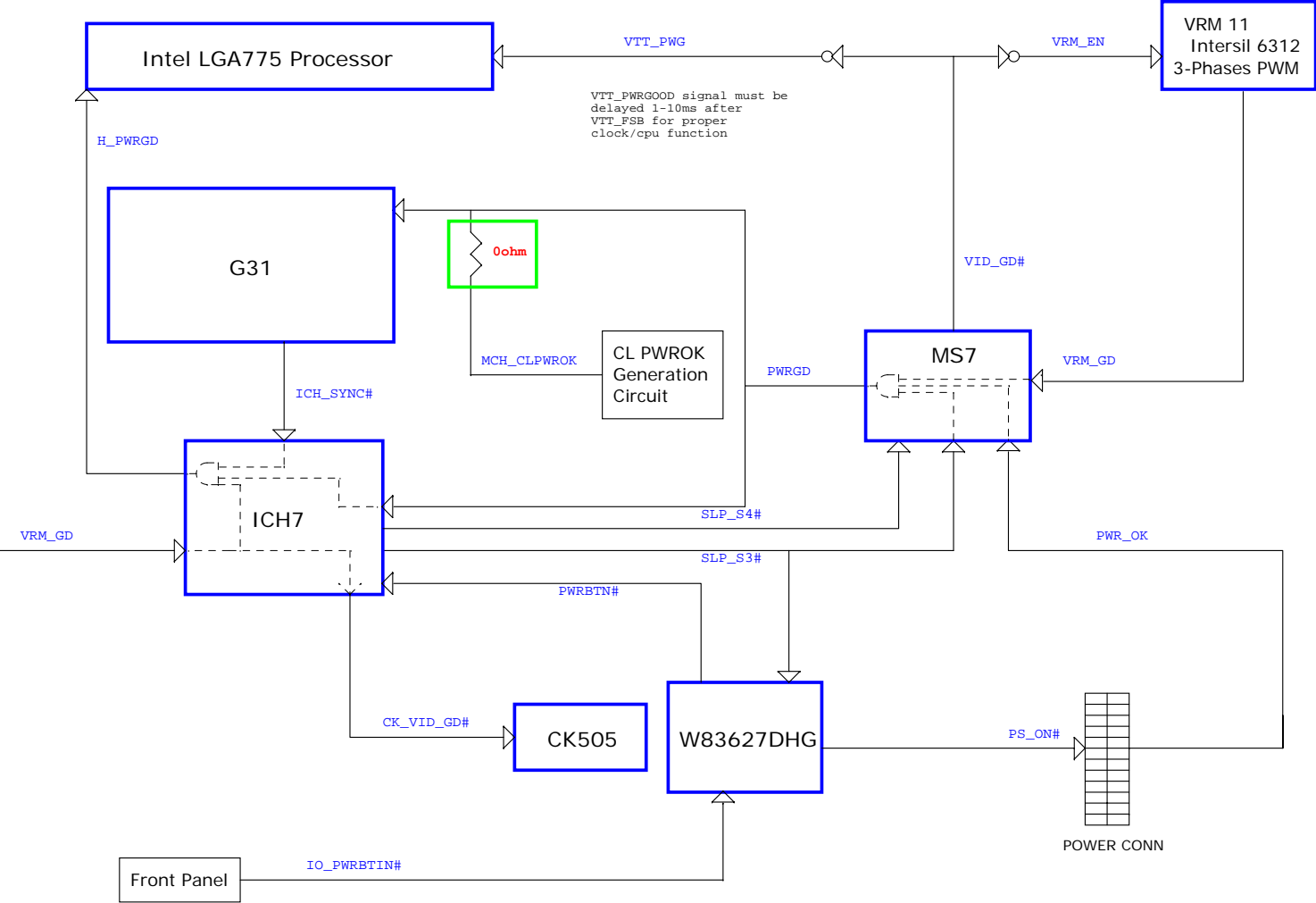
PS/2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

Micro Star Restricted Secret		
Title	Power Delivery	Rev 20
Document Number	MS-7407	
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CLOCK MAP



PWROK MAP



RESET MAP

